CUSTOMIZATION OF A RISC-V PROCESSOR TO ACHIEVE DSP PERFORMANCE GAIN
**Codasip Studio:**
- Introduced in 2014
- Silicon-proven by major vendors
- Allows for fast & easy customization of base instruction set:
  - Single cycle MAC
  - Floating point
  - Custom crypto functions
  - Non-standard data types
  - ... and many others

- Set the best ratio of power consumption and performance
- Easily add optional subsets and features
- Fine-tune the processor for intended application
- Differentiate and gain competitive advantage!
1. STEP: BK SELECTION

Selection of low-power, high-performance options for *any design*

The Berkelium series

Base versions:

- Bk1 – ultra-low cost option
- Bk3 – all-purpose
- Bk5 – best performance
- **Bk5-64** – high data bandwidth, energy efficient
  ➤ *64bit variant, new in November 2017!*

All fully **compliant** with the RISC-V specification

All fully **customizable**
2. STEP: ISA CONFIGURATION

I = integer ISA, 32 GPRs
E = integer ISA, 16 GPRs
M = multiplication extension
C = compressed instructions
F = floating-point ISA

p = parallel multiplier
d = JTAG debug
3. STEP: NEW INSTRUCTIONS

codix_berkelium - Profiling Result

- Executable: codix_berkelium
- Clock Cycles: 133061
- Sampling Rate: 1
- Project Name: codix_berkelium
- Studio Version: 6.8.1-2 win 7 EVALUATION
- Created: Monday, 2017-11-13 22:33:44

Resources Coverage

<table>
<thead>
<tr>
<th>Basic Resources</th>
<th>Read</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>r_csr_mepc</td>
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<tr>
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4. STEP: AUTOMATED GENERATION

Processor Modeling → Software analysis → SDK Synthesis → RTL Synthesis → Verification

- C/C++ Compiler
- Assembler
- Linker
- IA Simulator, Profiler, Debugger
- CA Simulator, Profiler, Debugger
- Reference Model
- RTL
- Universal Verification Methodology (UVM) Environment

- Codasip IP or User Specified Architecture in CodAL
- Instruction Accurate Model (IA)
- Cycle Accurate Model (CA)
THE MICROSEMI USE CASE: AUDIO PROCESSING SOLUTION FOR IOT

Requirements:

- Low power
- Low cost
- Possibility to create derivative designs to meet diverse requirements
- Reduced time-to-market
- Performance improvement
THE MICROSEMI USE CASE: STEPS

1. **STEP:** Berkelium core selection
   - Bk3

2. **STEP:** ISA configuration
   - Bk3-I = enabled integer instructions only
   - Bk3-IM = enabled multiplication/division instructions
   - Bk3-IM-p = enabled multiplication/division + parallel HW multiplier

3. **STEP:** new instructions
   - new DSP instructions

4. **STEP:** automated generation
   - SDK + RTL + UVM automatically generated for Bk3-IM-p + DSP
# The Microsemi Use Case: Results (Table)

- Performance improvement
- No advanced manufacturing processes
- No increase in clock frequency
- Took only 3 days

<table>
<thead>
<tr>
<th>Codasip RISC-V Processor</th>
<th>Clock Cycles</th>
<th>Code size</th>
<th>Area (Gates)</th>
<th>Difference against the lower configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bk-3 Base Configuration</td>
<td>1,764,256</td>
<td>232</td>
<td>16.0k</td>
<td>Speedup vs. RV32-I: 4.12x</td>
</tr>
<tr>
<td>Bk-3 Base + Serial Multiplier</td>
<td>427,561</td>
<td>148</td>
<td>19.7k</td>
<td>Speedup vs. RV32-IM: 4.12x</td>
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<tr>
<td>Bk-3 Base + Parallel Multiplier</td>
<td>133,061</td>
<td>148</td>
<td>26.2k</td>
<td>Speedup vs. RV32-IM: 13.26x</td>
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<tr>
<td>Bk-3 Base + DSP Extensions</td>
<td>31,371</td>
<td>64</td>
<td>38.7k</td>
<td>Speedup vs. RV32-IM: 56.24x</td>
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</tbody>
</table>

Design Iterations = 3 Days
THE MICROSEMI USE CASE: RESULTS (GRAPH)

Performance improvements for FIR filter using Studio*

* Implementing RISC-V for IoT applications, Dan Ganousis & Vijay Subramaniam, Design Automation Conference 2017
Thank you for your attention!

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