Andes Technology

- Taiwan-based CPU IP company with over 2.5-billion Andes-Embedded SoCs shipped in diverse applications.

- Taking RISC-V to those markets with the solutions we developed in the past 13 years.

- A major contributor to RISC-V tools such as GCC, binutils, newlib, and recently LLVM and LLD.
RISC-V DSP (P) Extension TG

- P extension task group charter
  - Define and ratify Packed-SIMD DSP extension instructions operating on XLEN-bit integer registers for embedded RISC-V processors.
  - Define compiler intrinsic functions that can be directly used in high-level programming languages.

- Chair: Chuan-Hua Chang, Andes Technology
- Co-chair: Richard Herveille, RoaLogic
RISC-V DSP (P) Extension Proposal

- DSP instruction set proposal based on AndeStar™ V3 DSP ISA.
  - User XLEN-bit GPRs.
  - Support saturation and rounding.
  - Support fixed-point and integer data types.
  - **SIMD**-instructions with 8b, 16b, 32b element size.
  - **Non-SIMD** DSP instructions operating on 16-bit, 32-bit and 64-bit data types.
  - 64-bit signed/unsigned addition & subtraction
  - 64-bit signed/unsigned multiplication & addition
    - E.g., 64 = 64 + 16x16 + 16x16 or
    - E.g., 64 = 64 + 32x32
16-Bit SIMD Instructions

- OP1
- OP2

Operations:
- Min
- Max
- Clip
- Compare
- Signed
- Unsigned

Operations:
- +
- *
- <<
- >>
- ABS
8-Bit SIMD Instructions

- Min
- Max
- Unpack
- ABS
- Signed
- Unsigned
Dual 16x16 & 32-Bit Add/Sub

6x v.s. Baseline
Dual 16x16 & 64-Bit Add/Sub

12x v.s. Baseline
GPR vs Separate Register

- GPR-based SIMD is a more efficient, low power DSP solution for embedded systems running applications in various domains such as audio/speech decoding and processing, IoT sensor data processing, wearable fitness devices, etc.
- It addresses the need for high performance generic code processing, as well as digital signal processing.
Ease of Use

- Provide data types and instructions that can be recognized and used by a compiler.
- Provide intrinsic functions for software developers to use the DSP instructions directly in C/C++ code.
- Provide optimized DSP libraries/middlewares covering common DSP functions and algorithms.
  - AndeStar™ V3 core performance: D10 is 79% faster than N10.
64-bit Data Type

- Use pairs of GPRs on RV32.
- Use a GPR on RV64.
- Needed for compiler to generate DSP instructions automatically.
- The 64-bit operand type is an interface specification. An implementation can still implement 2R1W register file with multi-cycle reads/writes to support the 64-bit type on RV32.
DSP ISA Performance

- Helix MP3 decoder

<table>
<thead>
<tr>
<th>GCC Compiler</th>
<th>Decode (MCPS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compile with 32b base ISA</td>
<td>22.64</td>
</tr>
<tr>
<td>Compile with 32b base+DSP ISA</td>
<td>10.35</td>
</tr>
<tr>
<td>Cycle reduction %</td>
<td>54%</td>
</tr>
<tr>
<td>Cycle % of 64b paired-GPR insts</td>
<td>~70%</td>
</tr>
</tbody>
</table>

- G.729 codec

<table>
<thead>
<tr>
<th></th>
<th>Encode (MCPS)</th>
<th>Decode (MCPS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler alone</td>
<td>95.45</td>
<td>26.83</td>
</tr>
<tr>
<td>Intrinsic + Compiler</td>
<td>26.31</td>
<td>6.02</td>
</tr>
<tr>
<td>Cycle reduction %</td>
<td>72%</td>
<td>78%</td>
</tr>
</tbody>
</table>

* MCPS: Millions of Cycles Per Second
### AMR-WB Performance

<table>
<thead>
<tr>
<th>AMR-WB</th>
<th>N10</th>
<th>D10</th>
<th>D15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Encode</td>
<td>282.93</td>
<td>59.64</td>
<td>41.32</td>
</tr>
<tr>
<td>Decode</td>
<td>63.76</td>
<td>15.50</td>
<td>10.93</td>
</tr>
</tbody>
</table>

- **N10**: Base ISA + 1-issue pipeline
- **D10**: Base + DSP ISA + 1-issue pipeline
- **D15**: Base + DSP ISA + 2-issue pipeline

The benchmarking numbers are in MCPS. (Million Cycle Per Second)
For all the test vectors, the average (AVG) numbers are concluded.
ANSI-C Code for the AMR-WB speech codec:
[http://www.etsi.org/deliver/etsi_ts/126100_126199/126173/14.00.00_60/ts_126173v140000p0.zip](http://www.etsi.org/deliver/etsi_ts/126100_126199/126173/14.00.00_60/ts_126173v140000p0.zip)
DSP Library Performance Speedup

- Average speedup: 1.79x
- Maximum speedup: 5.51x
In the process of discussion with Technical Committee Chair and Co-chair to create the task group.

After the task group is created, TG will arrange bi-weekly meetings and publicly invite people to participate.
Thank You!

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