The State of RISC-V Software

Palmer Dabbelt: RISC-V Software Team Lead at SiFive, Software Group Vice Chair at RISC-V Foundation
Arun Thomas: Engineer at Draper Labs, Software Group Chair at RISC-V Foundation
RISC-V Workshop in Barcelona, May 2018

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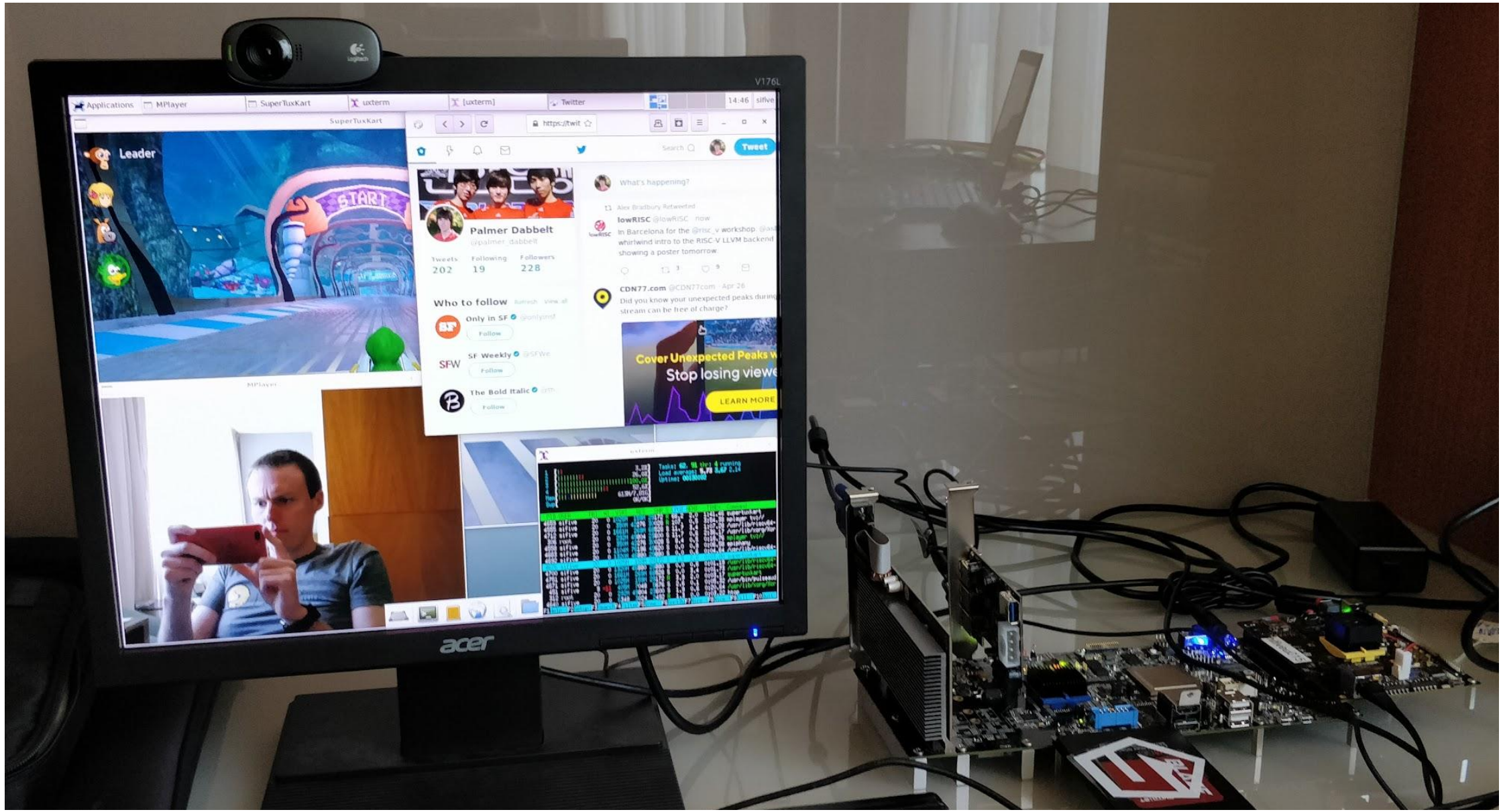
The State of RISC-V Software



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GNU-Based Toolchains

- **binutils, GCC: May, 2017**
- **glibc: February, 2018**
  - only supports rv64i-based ISAs
- **newlib: August, 2017**
- **“Probably not a compiler bug”**

bluespec

redhat

ANDES
TECHNOLOGY

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SiFive

bluespec

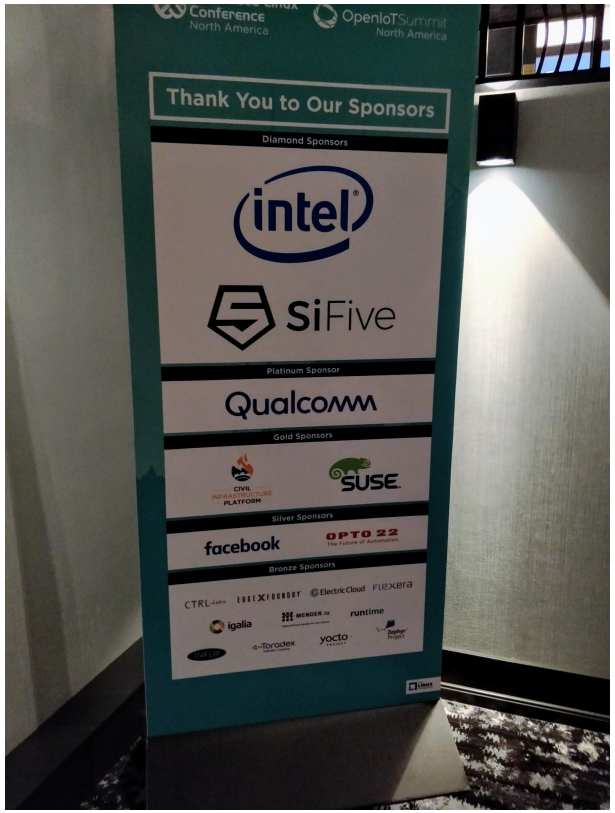
redhat

ANDES TECHNOLOGY

E31	Cortex-M3	Cortex-M4
RV32IAC M + U Modes	ARMv7-M, Thumb, Thumb-2	ARMv7-M, Thumb, Thumb-2
Up to 1.5 GHz in 28nm	Not Publicly Available	Not Publicly Available
1.61 DMIPS/MHz	1.25 DMIPS/MHz	1.25 DMIPS/MHz

RISC-V Linux Kernel Port

- **Linux: January, 2018**
  - Only RV64I-based systems
  - Drivers are trickling in now



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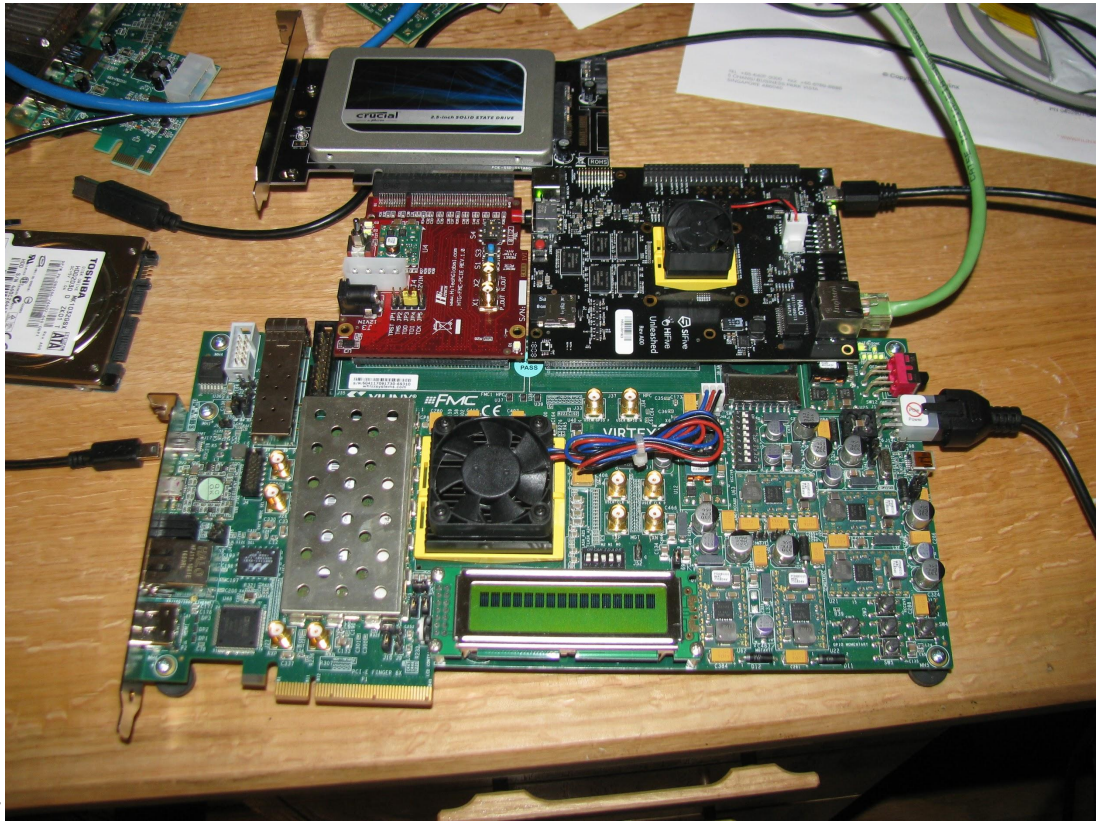
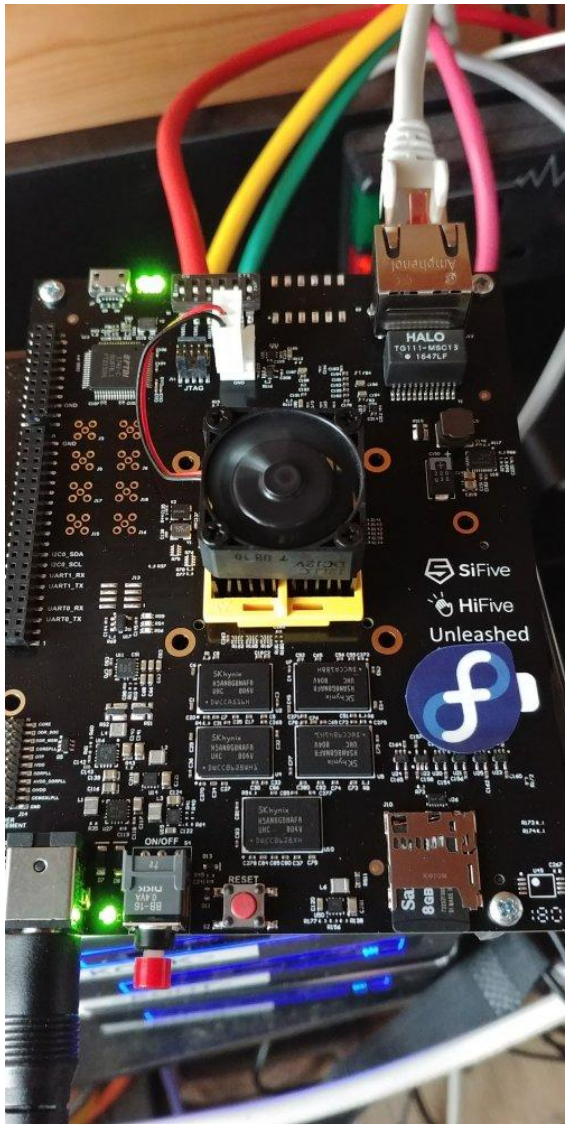
GNU/Linux Userspace: Fedora

redhat

- RISC-V Fedora Port in Progress
- Reproduced open-source FPGA shell
  - http://github.com/sifive/freedom
- Talk on Tuesday afternoon





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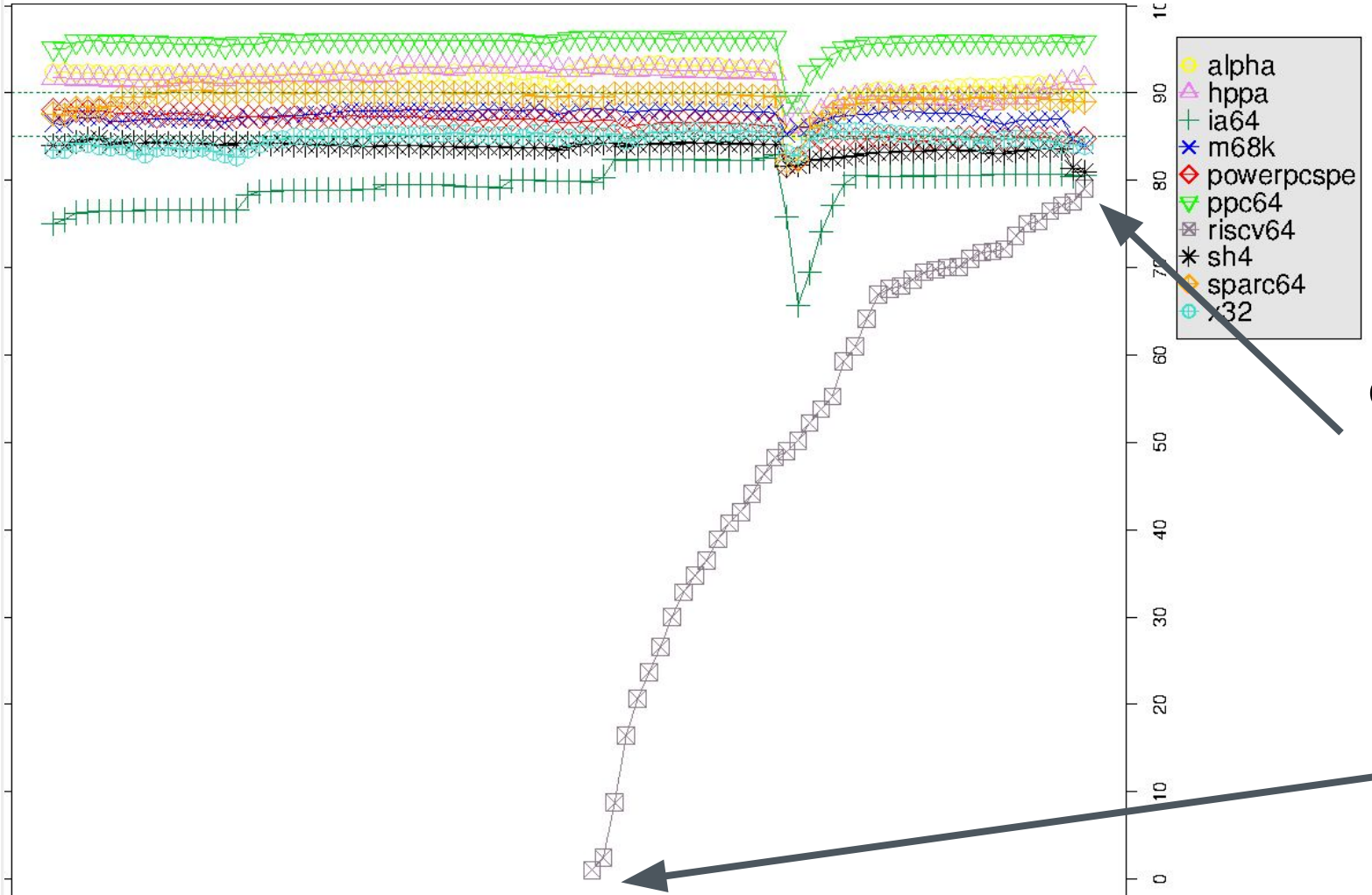
GNU/Linux Userspace: Debian

SiFive

- 80% of packages build! (about 40000)
- Talk on Thursday afternoon



debian

RISC-V LLVM Porting Effort

- **Alex Bradbury is in charge of RISC-V LLVM**
  - Talk yesterday afternoon
  - Poster on Tuesday night
- **RV32IM[A]FD support upstream**
  - Missing hard-float calling convention
  - Missing 64-bit support
  - Missing compressed support
- **Clang, Go, and OpenJDK have run code**
  - Rust port in progress
  - Poster on Tuesday

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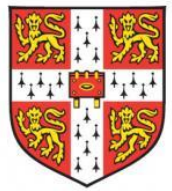
RISC-V FreeBSD Port

- Upstream since early 2016
- Latest RISC-V Privileged Spec
- Demonstrated booting on HW



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FreeBSD FOUNDATION

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Firmware for Application Cores

- **Berkeley Boot Loader (BBL)**
  - Boots, but not what we want
- **U-Boot is upstream**
  - RV32I-based Andes NX25 supported
- **TianoCore port in progress**
  - Abner Chang from HPE
- **CoreBoot RISC-V support is upstream, out of date**
  - Upstream since 2014!
- **UEFI standards process in process**

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Embedded Runtimes on RISC-V

- **Zephyr is upstream**
  - https://github.com/zephyrproject-rtos/zephyr/tree/master/arch/riscv32
- **seL4 port upstream since April, 2018**
  - https://sel4.systems/pipermail/devel/2018-April/001928.html
- **FreeRTOS exists, not upstream yet**
- **Micrium uC/OS**
  - https://github.com/RISCV-on-Microsemi-FPGA/uCOS
- **ThreadX**
  - https://content.riscv.org/wp-content/uploads/2017/12/Tue1512-ThreadX-for-RISC-V-Draft-3.2.pdf

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Debugging RISC-V Software

- **RISC-V External Debug Specification**
  - Thanks to Megan Wachs at SiFive, who is running the task group
- **GDB port is upstream, not yet released**
  - Thanks to Andrew Burgess from Embecosm
  - Talk on Tuesday
- **RISC-V OpenOCD port exists, not upstream**
  - Not in good shape
- **Lots of commercial adoption!**
  - Seggar and Lauterbach support RISC-V -- talk and poster on Tuesday
  - UltraSOC supports multiple core vendors
  - IAR support is coming

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Open Standards Work!

- Kito Cheng (Andes Technology): GCC and newlib
- Jim Wilson (SiFive): binutils and GCC
- Darius Rad (Bluespec): glibc
- Andrew Waterman (SiFive): binutils, GCC, and glibc
- DJ Delorie (RedHat): glibc

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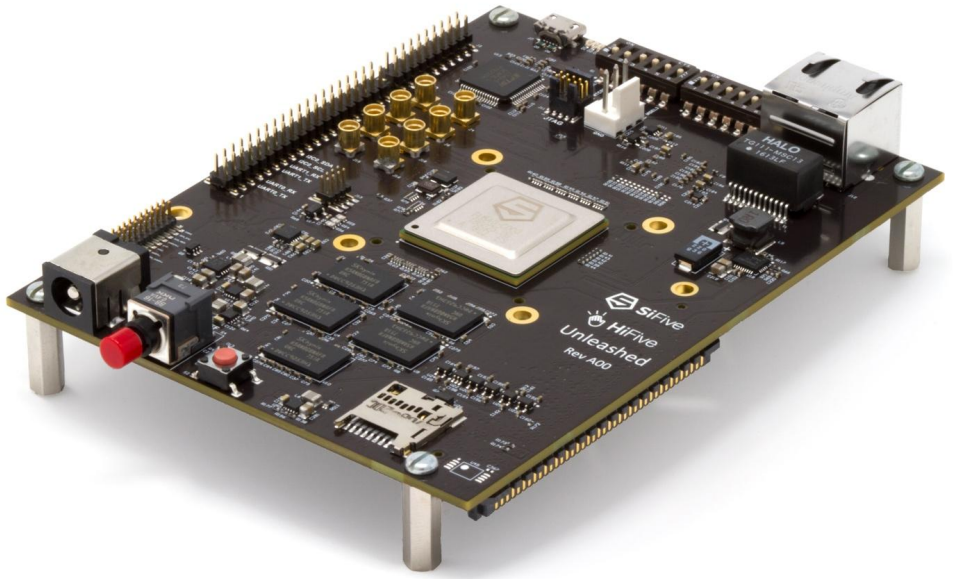
HiFive Unleashed

- **SiFive FU540-C000 (built in 28nm)**
  - 4+1 Multi-Core Coherent Configuration
  - 4x U54 RV64GC Application Cores with Sv39
  - Virtual Memory Support
  - 1x E51 RV64IMAC Management Core
  - Coherent 2MB L2 Cache
  - 1x Gigabit Ethernet
- **8 GB 64-bit DDR4 with ECC**
- **Gigabit Ethernet Port**
- **32 MB Quad SPI Flash**
- **MicroSD card for removable storage**
- **Expansion via FMC connector**
- **More during Yunsup's talk**



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RISC-V Software Implementations

- Spike: a simple RISC-V software implementation
  - https://github.com/riscv/riscv-isa-sim
- RV8: A Fast RISC-V JIT
- Renode: IoT focused simulator
- QEMU: the standard full-system simulator
  - https://www.sifive.com/blog/2017/12/20/risc-v-qemu-part-1-privileged-isa-hifive1-virtio/
  - https://www.sifive.com/blog/2018/04/25/risc-v-qemu-part-2-the-risc-v-qemu-port-is-upstream/

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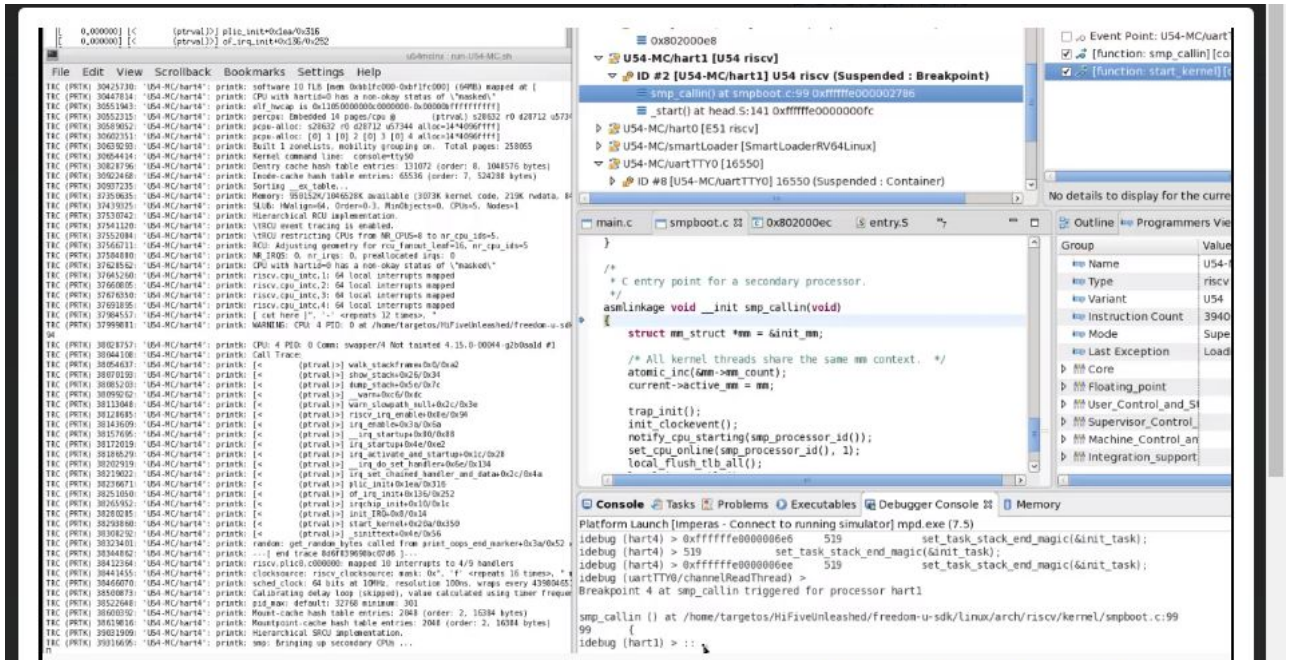
Commercial RISC-V Simulators

- **Imperas OVP**
  - Boots Linux in 10s
  - Supports SMP
  - Matches HiFive Unleashed
- **Esperanto Simulator**
  - Fast JITing simulator



imperas

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What's Next?

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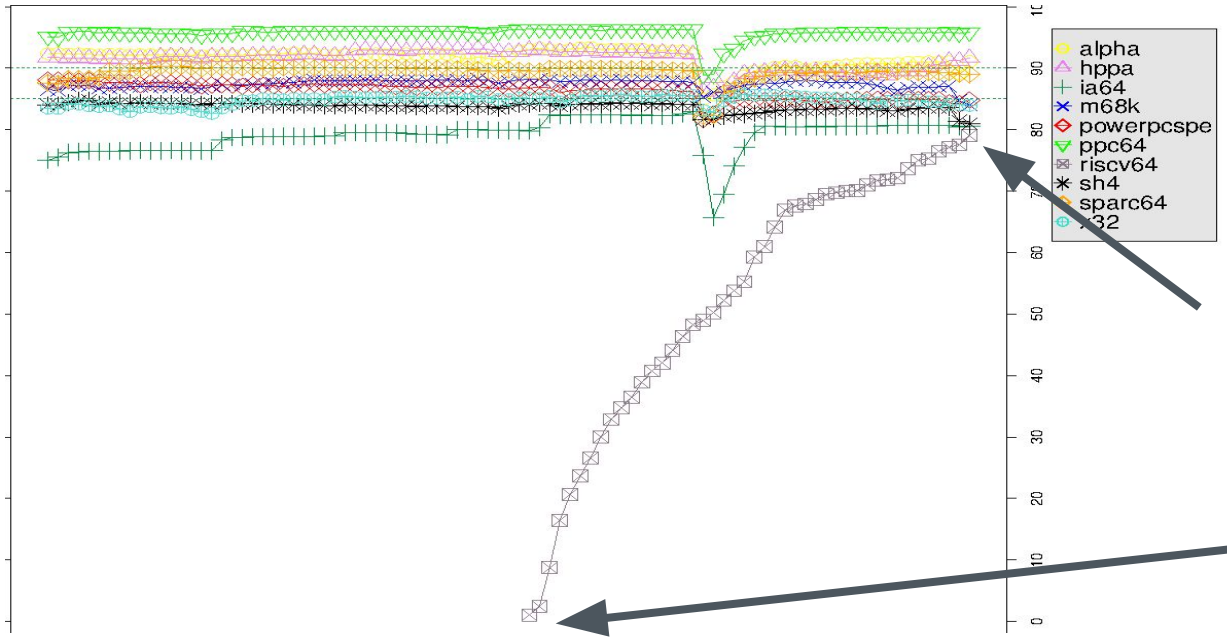
Linux Distributions



80%
May

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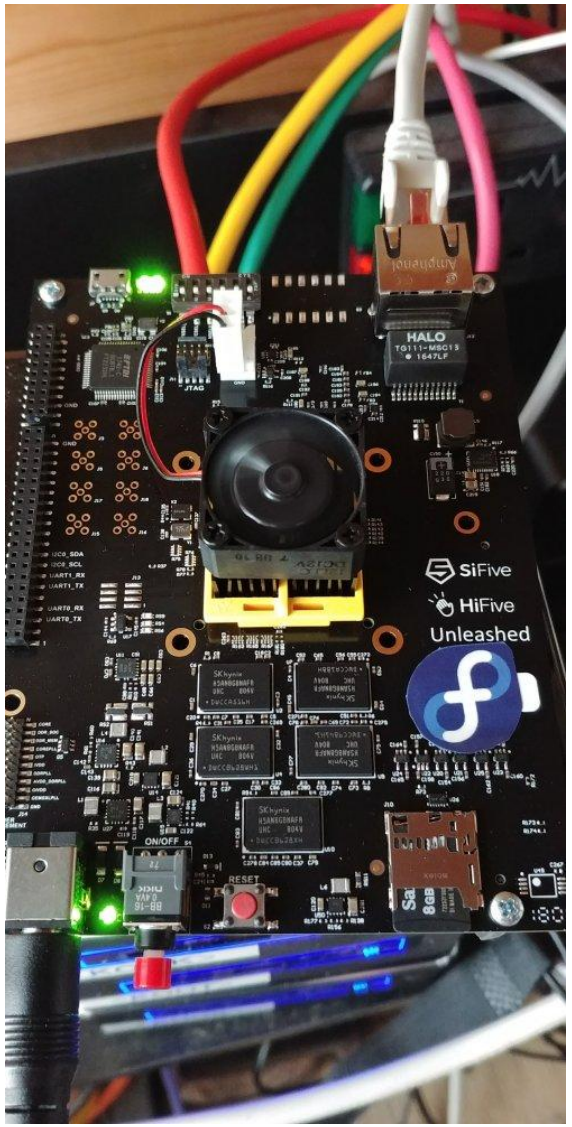
March



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Developers!

```
$ git log arch/riscv/ | grep ^Author | sort | uniq | wc -l
22
$ git log arch/mips/ | grep ^Author | sort | uniq | wc -l
895
$ git log arch/arm64/ | grep ^Author | sort | uniq | wc -l
814
$ git log arch/x86/ | grep ^Author | sort | uniq | wc -l
1880
```


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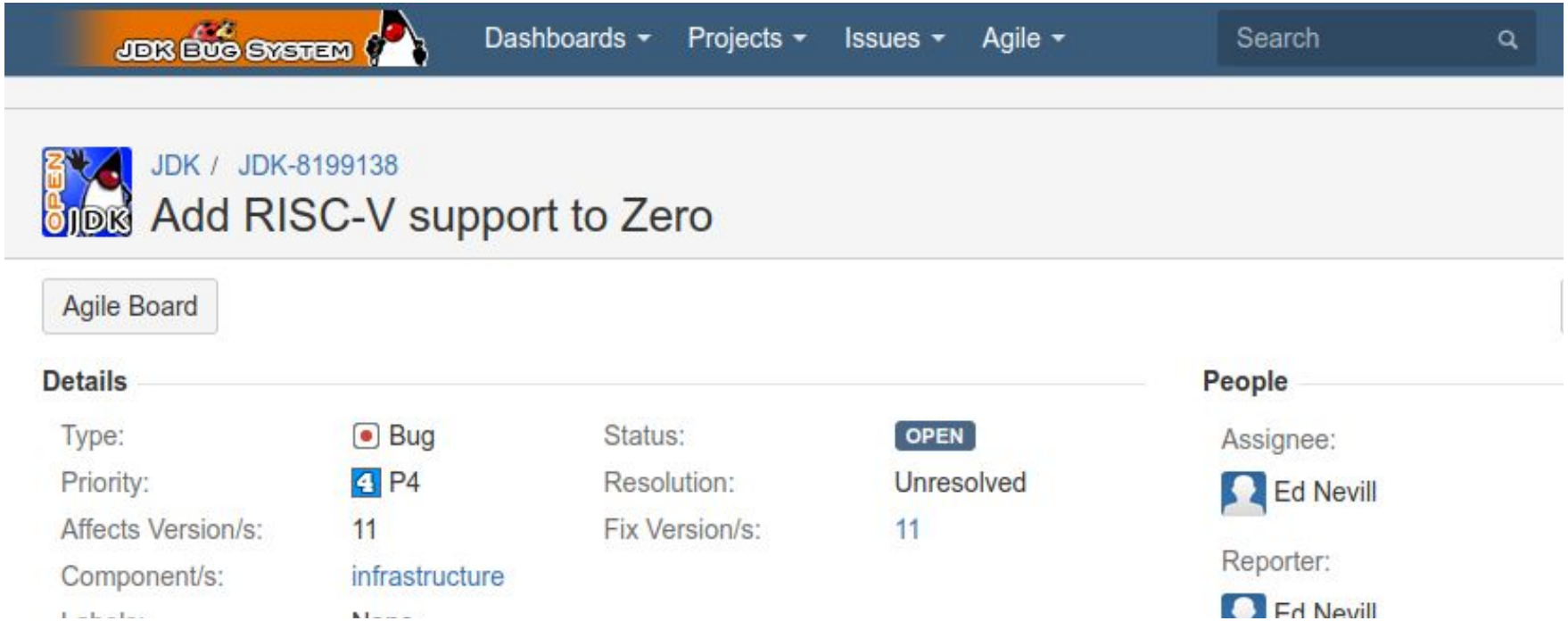
High Performance Java on RISC-V

- Patch for Zero interpreter
- Need a high-performance JIT
- J extension working group
- Boris Shingarov has a poster



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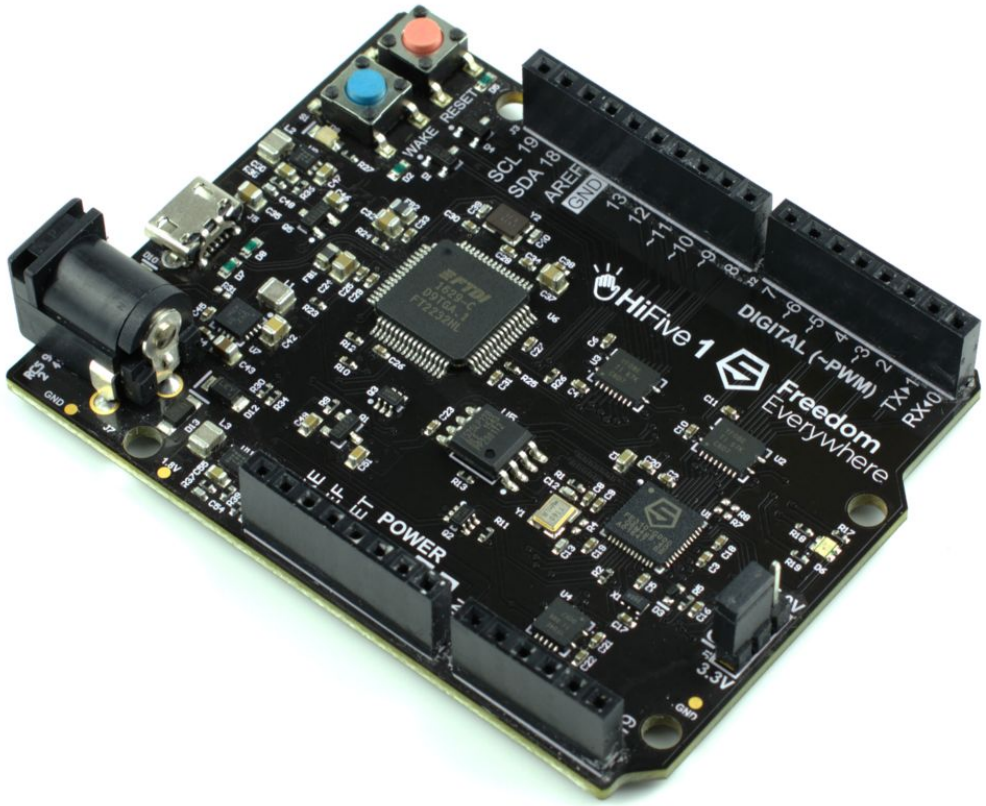
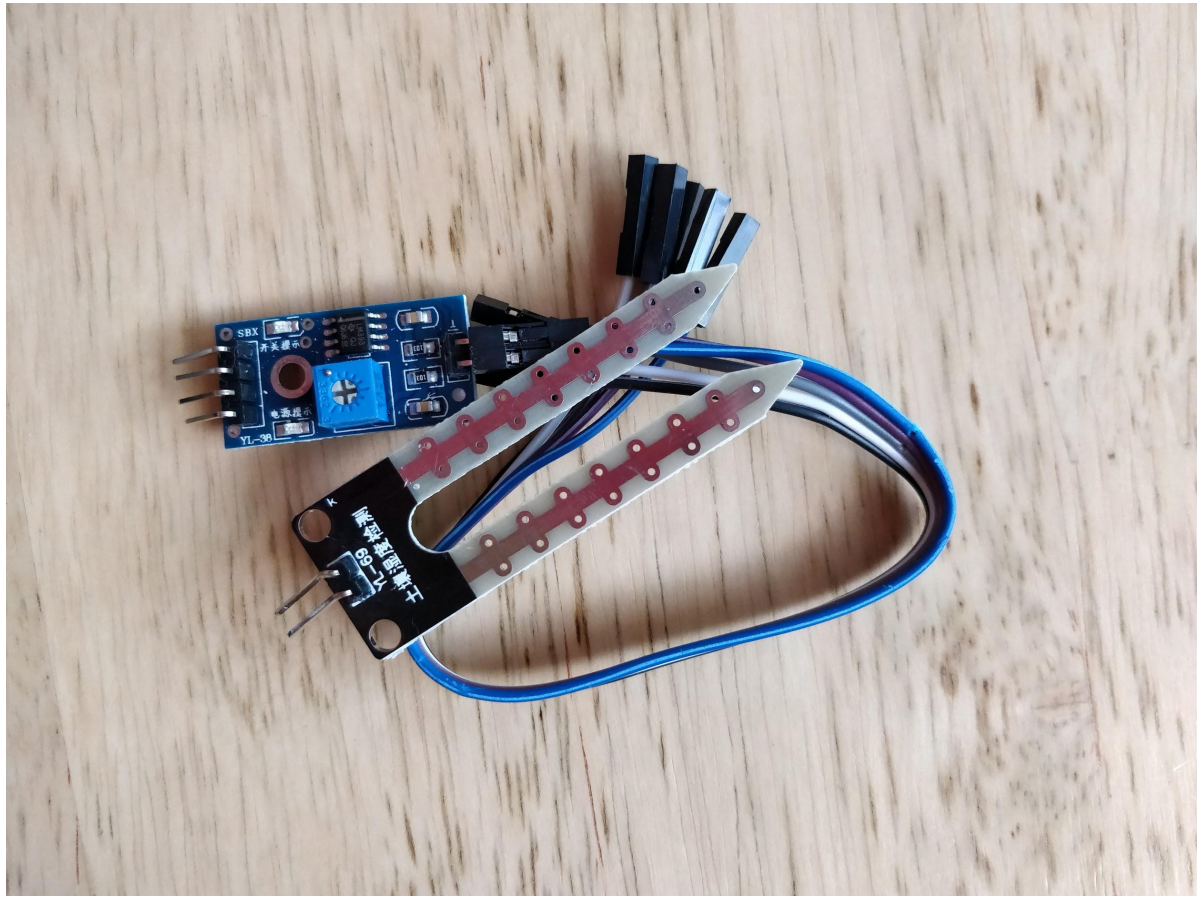
Arduino Runtime on RISC-V





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RISC-V Support on Platform.IO

```
[Tue Apr 17 16:19:44 2018] Processing freedom-e300-hifive1 (platform: riscv; board: freedom-e300-hifive1; framework: freedom-e-sdk)
------------------------------------------------------------------------------------------------------------------------
Verbose mode can be enabled via `-v, --verbose` option
PLATFORM: RISC-V > HiFive1
SYSTEM: FE310 320MHz 16KB RAM (16MB Flash)
DEBUG: CURRENT(ftdi) ON-BOARD(ftdi)
Library Dependency Finder -> http://bit.ly/configure-pio-ldf
LDF MODES: FINDER(chain) COMPATIBILITY(light)
Collected 0 compatible libraries
Scanning dependencies...
No dependencies
Calculating size .pioenvs/freedom-e300-hifive1/firmware.elf
text       data     bss     dec     hex filename
52754      2512    2332   57598    e0fe .pioenvs/freedom-e300-hifive1/firmware.elf
================================================== [SUCCESS] Took 0.45 seconds ==================================================

[Tue Apr 17 16:19:45 2018] Processing coreplexip-e31-arty (platform: riscv; board: coreplexip-e31-arty; framework: freedom-e-sdk)
------------------------------------------------------------------------------------------------------------------------
Verbose mode can be enabled via `-v, --verbose` option
PLATFORM: RISC-V > Freedom E310 Arty (Artix-7) FPGA Dev Kit
SYSTEM: FE310 1500MHz 256MB RAM (16MB Flash)
DEBUG: CURRENT(olimex-arm-usb-tiny-h) EXTERNAL(olimex-arm-usb-tiny-h)
Library Dependency Finder -> http://bit.ly/configure-pio-ldf
LDF MODES: FINDER(chain) COMPATIBILITY(light)
Collected 0 compatible libraries
Scanning dependencies...
No dependencies
Calculating size .pioenvs/coreplexip-e31-arty/firmware.elf
text       data     bss     dec     hex filename
3340       1080    2172    6592    19c0 .pioenvs/coreplexip-e31-arty/firmware.elf
================================================== [SUCCESS] Took 0.44 seconds ==================================================

============================================================ [SUMMARY] ============================================================
Environment freedom-e300-hifive1        [SUCCESS]
Environment coreplexip-e31-arty         [SUCCESS]
================================================== [SUCCESS] Took 0.89 seconds ==================================================
```


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RISC-V Platform Spec Working Group

- **Defines profiles for types of RISC-V systems**
  - Bare-Metal Embedded
  - RTOS
  - Embedded Linux
  - Portable Linux

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- **Very important**
- **Needs to happen**
- **Time to take this seriously**

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- **Needs to happen**
- **Time to take this seriously**
- **Looking for a chair**

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Getting Involved

- **Upstream!**
  - Use a project's regular communication mechanisms
- **Specific to RISC-V**
  - https://github.com/riscv/: Contains in-progress ports
  - sw-dev@groups.riscv.org: Software discussion
  - patches@groups.riscv.org: Patches to RISC-V ports
  - #riscv on Freenode: General RISC-V discussion
  - linux-riscv@lists.infradead.org: RISC-V Linux Port
- **Selected Projects**
  - RV32I support in Linux and glibc
  - RV64I support for U-Boot, Zephyr, FreeRTOS, etc
- **Help with the RISC-V Platform Specification**
- **Beta Program for Open Source Developers: info@sifive.com**

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