The State of RISC-V Software

Palmer Dabbelt: RISC-V Software Team Lead at SiFive, Software Group Vice Chair at RISC-V Foundation
Arun Thomas: Engineer at Draper Labs, Software Group Chair at RISC-V Foundation
RISC-V Workshop in Barcelona, May 2018
The State of RISC-V Software
GNU-Based Toolchains

- **binutils, GCC: May, 2017**
- **glibc: February, 2018**
  - only supports rv64i-based ISAs
- **newlib: August, 2017**
- "Probably not a compiler bug"
GNU-Based Toolchains

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**SiFive**

<table>
<thead>
<tr>
<th>E31</th>
<th>Cortex-M3</th>
<th>Cortex-M4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RV32IAC</td>
<td>ARMv7-M, Thumb, Thumb-2</td>
<td>ARMv7-M, Thumb, Thumb-2</td>
</tr>
<tr>
<td>M + U Modes</td>
<td>Not Publicly Available</td>
<td>Not Publicly Available</td>
</tr>
<tr>
<td>Up to 1.5 GHz in 28nm</td>
<td>1.25 DMIPS/MHz</td>
<td>1.25 DMIPS/MHz</td>
</tr>
<tr>
<td><strong>1.61 DMIPS/MHz</strong></td>
<td></td>
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</tbody>
</table>
RISC-V Linux Kernel Port

- **Linux: January, 2018**
  - Only RV64I-based systems
  - Drivers are trickling in now
GNU/Linux Userspace: Fedora

- RISC-V Fedora Port in Progress
- Reproduced open-source FPGA shell
  - http://github.com/sifive/freedom
- Talk on Tuesday afternoon
GNU/Linux Userspace: Debian

- 80% of packages build! (about 40000)
- Talk on Thursday afternoon
RISC-V LLVM Porting Effort

- Alex Bradbury is in charge of RISC-V LLVM
  - Talk yesterday afternoon
  - Poster on Tuesday night
- RV32IM[A]FD support upstream
  - Missing hard-float calling convention
  - Missing 64-bit support
  - Missing compressed support
- Clang, Go, and OpenJDK have run code
  - Rust port in progress
  - Poster on Tuesday
RISC-V FreeBSD Port

- Upstream since early 2016
- Latest RISC-V Privileged Spec
- Demonstrated booting on HW
Firmware for Application Cores

- Berkeley Boot Loader (BBL)
  - Boots, but not what we want
- U-Boot is upstream
  - RV32I-based Andes NX25 supported
- TianoCore port in progress
  - Abner Chang from HPE
- CoreBoot RISC-V support is upstream, out of date
  - Upstream since 2014!
- UEFI standards process in process
Embedded Runtimes on RISC-V

- **Zephyr is upstream**

- **seL4 port upstream since April, 2018**

- **FreeRTOS exists, not upstream yet**

- **Micrium uC/OS**
  - [https://github.com/RISCV-on-Microsemi-FPGA/uCOS](https://github.com/RISCV-on-Microsemi-FPGA/uCOS)

- **ThreadX**
Debugging RISC-V Software

- **RISC-V External Debug Specification**
  - Thanks to Megan Wachs at SiFive, who is running the task group
- **GDB port is upstream, not yet released**
  - Thanks to Andrew Burgess from Embecosm
  - Talk on Tuesday
- **RISC-V OpenOCD port exists, not upstream**
  - Not in good shape
- **Lots of commercial adoption!**
  - Seggar and Lauterbach support RISC-V -- talk and poster on Tuesday
  - UltraSOC supports multiple core vendors
  - IAR support is coming
Open Standards Work!

- Kito Cheng (Andes Technology): GCC and newlib
- Jim Wilson (SiFive): binutils and GCC
- Darius Rad (Bluespec): glibc
- Andrew Waterman (SiFive): binutils, GCC, and glibc
- DJ Delorie (RedHat): glibc
HiFive Unleashed

- SiFive FU540-C000 (built in 28nm)
  - 4+1 Multi-Core Coherent Configuration
  - 4x U54 RV64GC Application Cores with Sv39
  - Virtual Memory Support
  - 1x E51 RV64IMAC Management Core
  - Coherent 2MB L2 Cache
  - 1x Gigabit Ethernet
- 8 GB 64-bit DDR4 with ECC
- Gigabit Ethernet Port
- 32 MB Quad SPI Flash
- MicroSD card for removable storage
- Expansion via FMC connector
- More during Yunsup’s talk
RISC-V Software Implementations

- **Spike**: a simple RISC-V software implementation
  - [https://github.com/riscv/riscv-isa-sim](https://github.com/riscv/riscv-isa-sim)
- **RV8**: A Fast RISC-V JIT
- **Renode**: IoT focused simulator
- **QEMU**: the standard full-system simulator
  - [https://www.sifive.com/blog/2017/12/20/risc-v-qemu-part-1-privileged-isa-hifive1-virtio/](https://www.sifive.com/blog/2017/12/20/risc-v-qemu-part-1-privileged-isa-hifive1-virtio/)
Commercial RISC-V Simulators

- Imperas OVP
  - Boots Linux in 10s
  - Supports SMP
  - Matches HiFive Unleashed
- Esperanto Simulator
  - Fast JITing simulator
What’s Next?
Linux Distributions

80% May
0% March
Developers!

$ git log arch/riscv/ | grep ^Author | sort | uniq | wc -l
  22
$ git log arch/mips/ | grep ^Author | sort | uniq | wc -l
  895
$ git log arch/arm64/ | grep ^Author | sort | uniq | wc -l
  814
$ git log arch/x86/ | grep ^Author | sort | uniq | wc -l
  1880
High Performance Java on RISC-V

- Patch for Zero interpreter
- Need a high-performance JIT
- J extension working group
- Boris Shingarov has a poster
Arduino Runtime on RISC-V
RISC-V Support on Platform.IO


Verbose mode can be enabled via `-v, --verbose` option
PLATFORM: RISC-V > HiFive1
SYSTEM: EE310 320MHz 10KB RAM (10MB Flash)
DEBUG: CURRENT(ftdi) ON-BOARD(ftdi)
LDF MODES: FINDER(chain) COMPATIBILITY(light)
Collected 0 compatible libraries
Scanning dependencies...
No dependencies
Calculating size .pioenvs/freedom-e300-hifive1/firmware.elf
text  data  bss  dec  hex  filename
52754  2512  2332  57598  e8fe .pioenvs/freedom-e300-hifive1/firmware.elf
================================================================================ [SUCCESS] Took 6.45 seconds


Verbose mode can be enabled via `-v, --verbose` option
PLATFORM: RISC-V > Freedom E310 Arty (Artix-7) FPGA Dev Kit
SYSTEM: EE310 1560MHz 250MB RAM (16MB Flash)
DEBUG: CURRENT(olimex-arm-usb-tiny-h) EXTERNAL(olimex-arm-usb-tiny-h)
LDF MODES: FINDER(chain) COMPATIBILITY(light)
Collected 0 compatible libraries
Scanning dependencies...
No dependencies
Calculating size .pioenvs/coreplexip-e31-arty/firmware.elf
text  data  bss  dec  hex  filename
33460  1050  2172  6592  19c9 .pioenvs/coreplexip-e31-arty/firmware.elf
================================================================================ [SUCCESS] Took 6.44 seconds

Environment freedom-e300-hifive1 [SUCCESS]
Environment coreplexip-e31-arty [SUCCESS]
================================================================================ [SUMMARY] ==================================================================
Environment freedom-e300-hifive1 [SUCCESS]
Environment coreplexip-e31-arty [SUCCESS]
================================================================================ [SUCCESS] Took 8.89 seconds
RISC-V Platform Spec Working Group

- Defines profiles for types of RISC-V systems
  - Bare-Metal Embedded
  - RTOS
  - Embedded Linux
  - Portable Linux
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- Very important
- Needs to happen
- Time to take this seriously
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- Looking for a chair
Getting Involved

● **Upstream!**
  ○ Use a project’s regular communication mechanisms

● **Specific to RISC-V**
  ○ [https://github.com/riscv/](https://github.com/riscv/): Contains in-progress ports
  ○ [sw-dev@groups.riscv.org](mailto:sw-dev@groups.riscv.org): Software discussion
  ○ [patches@groups.riscv.org](mailto:patches@groups.riscv.org): Patches to RISC-V ports
  ○ [#riscv on Freenode](https://freenode.net): General RISC-V discussion
  ○ [linux-riscv@lists.infradead.org](mailto:linux-riscv@lists.infradead.org): RISC-V Linux Port

● **Selected Projects**
  ○ RV32I support in Linux and glibc
  ○ RV64I support for U-Boot, Zephyr, FreeRTOS, etc

● **Help with the RISC-V Platform Specification**

● **Beta Program for Open Source Developers:** [info@sifive.com](mailto:info@sifive.com)