RISC-V: Enabling a New Era of Open Data-Centric Computing Architectures

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Forward-Looking Statements
Safe Harbor | Disclaimers

This presentation contains certain forward-looking statements that involve risks and uncertainties, including, but not limited to, statements regarding: the RISC-V Foundation and its initiatives; our contributions to and investments in the RISC-V ecosystem; the transition of our devices, platforms and systems to RISC-V architectures; shipments of RISC-V processor cores; our business strategy, growth opportunities and technology development efforts; market trends and data growth and its drivers. Forward-looking statements should not be read as a guarantee of future performance or results, and will not necessarily be accurate indications of the times at, or by, which such performance or results will be achieved, if at all. Forward-looking statements are subject to risks and uncertainties that could cause actual performance or results to differ materially from those expressed in or suggested by the forward-looking statements.

Additional key risks and uncertainties include the impact of continued uncertainty and volatility in global economic conditions; actions by competitors; business conditions; growth in our markets; and pricing trends and fluctuations in average selling prices. More information about the other risks and uncertainties that could affect our business are listed in our filings with the Securities and Exchange Commission (the "SEC") and available on the SEC's website at www.sec.gov, including our most recently filed periodic report, to which your attention is directed. We do not undertake any obligation to publicly update or revise any forward-looking statement, whether as a result of new information, future developments or otherwise, except as otherwise required by law.

The Evolving Role of Data
Creating the data-driven economy

Richness →

Data as a record	Data as communication	Data as efficiency	Data as currency

Value →
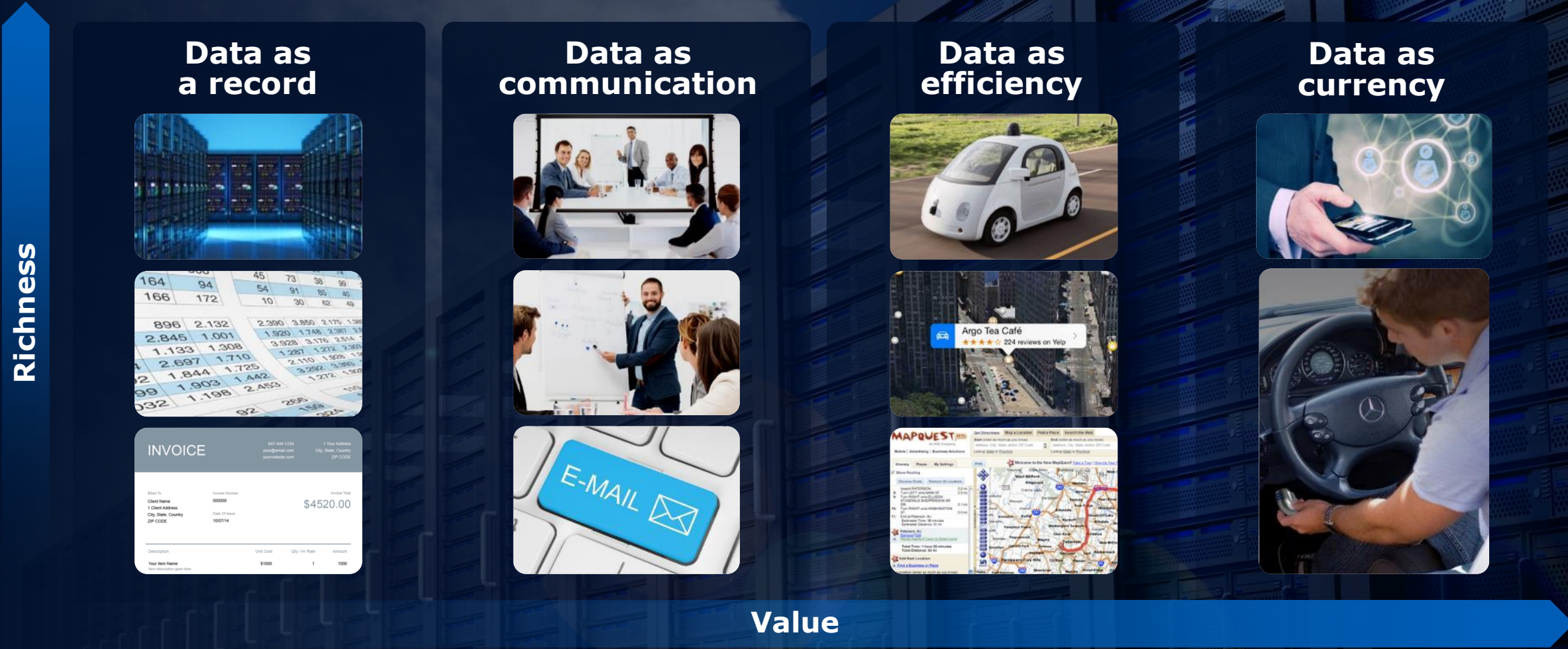
Diverse and Connected Data Types

Tight coupling between Big Data and Fast Data

Big Data
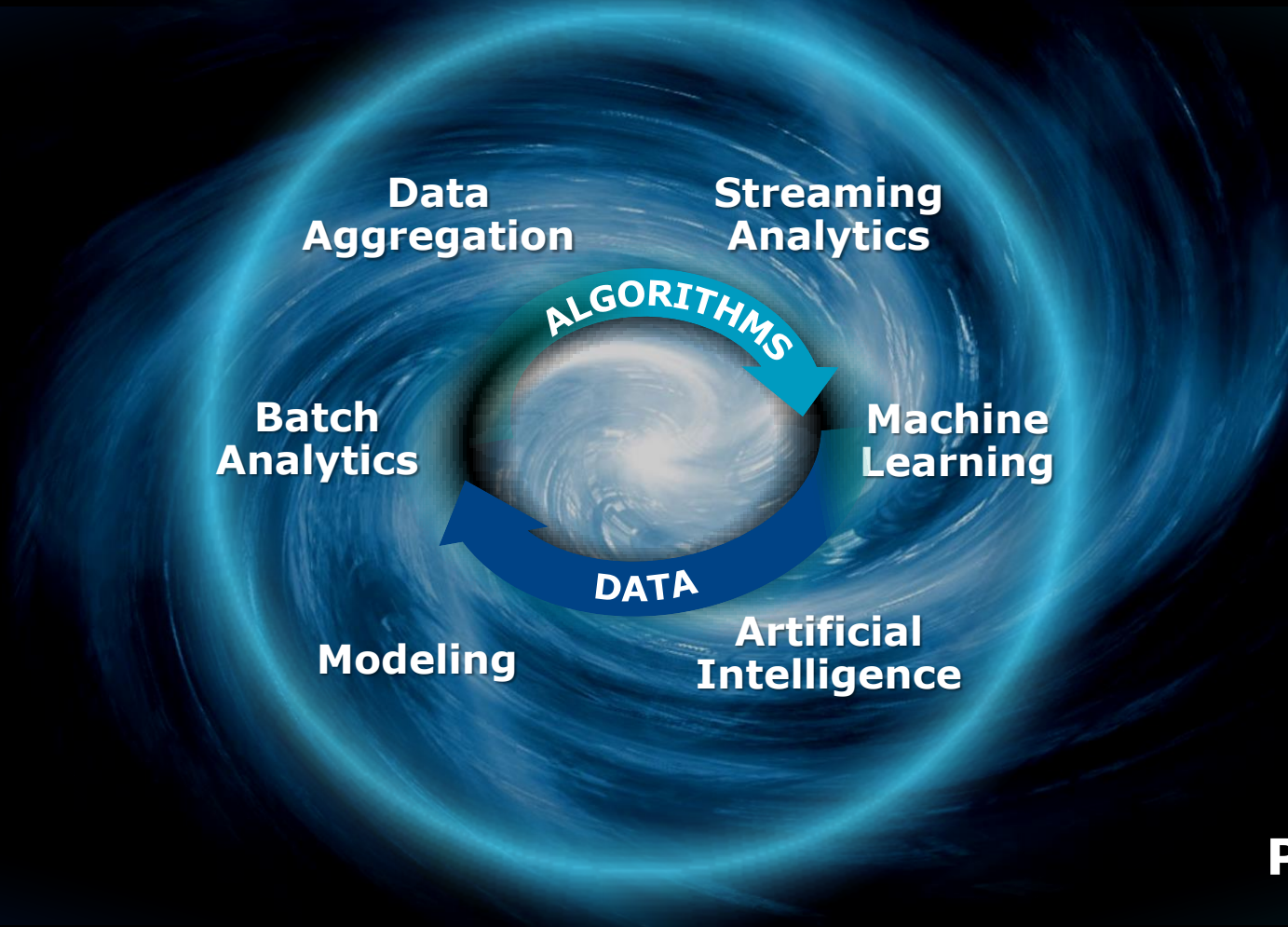
Insight

Prediction

Prescription

Scale

Data Aggregation

Streaming Analytics

ALGORITHMS

Batch Analytics

Machine Learning

DATA

Modeling

Artificial Intelligence

Fast Data

Mobility

Real-time Results

Smart Machines

Performance

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From General Purpose to Purpose Built

Architectures designed for Big Data, Fast Data applications

Big Data ← Expanding applications and workloads → **Fast Data**

General purpose
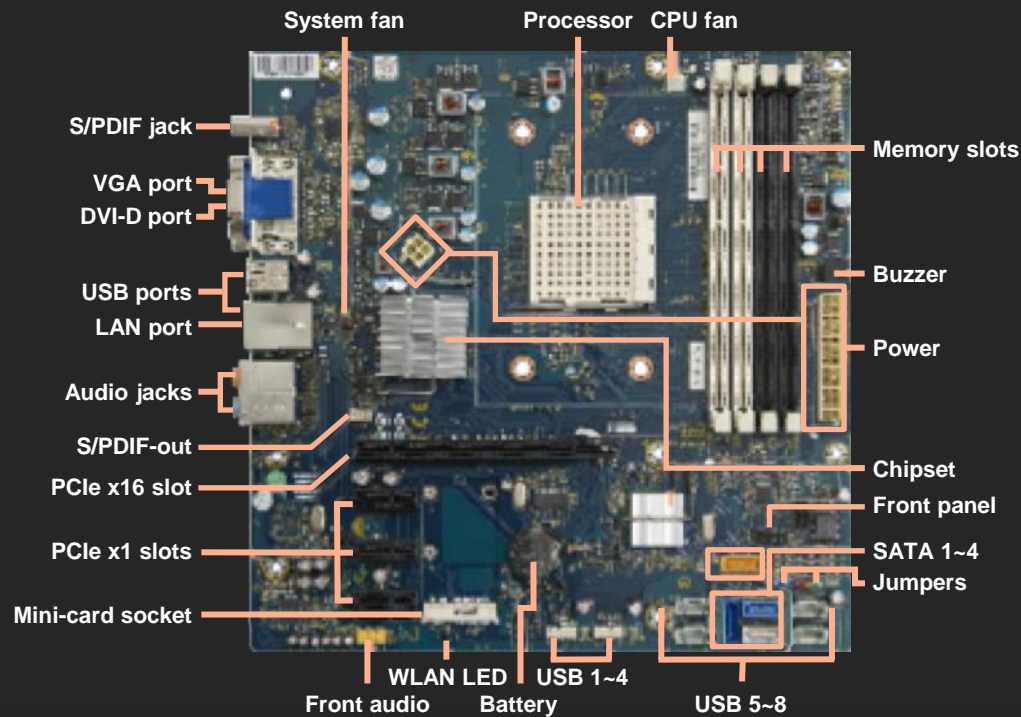compute-centric architecture

Solutions

Systems

Platforms

Devices

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5

General Purpose Architectures No Longer Sufficient

Big Data and Fast Data workloads exceed capability of uniform resource ratios

General Purpose Compute Architecture

- System fan
- Processor
- CPU fan
- S/PDIF jack
- VGA port
- DVI-D port
- Memory slots
- USB ports
- LAN port
- Buzzer
- Power
- Audio jacks
- S/PDIF-out
- PCIe x16 slot
- Chipset
- Front panel
- PCIe x1 slots
- SATA 1~4
- Jumpers
- Mini-card socket
- WLAN LED
- USB 1~4
- Front audio
- Battery
- USB 5~8

- Predetermined ratios of:
  – OS/App Processor
  – Specialty Processor
  – Memory
  – Storage
  – Interconnect
- Overhead of "PC" logic
- CPU-centric

Western Digital RISC-V Core

|	
PIC	RV32IMC
Debug	
Power Mgmt	Write Buffer
	I$
	D$
	Bus Interface Unit
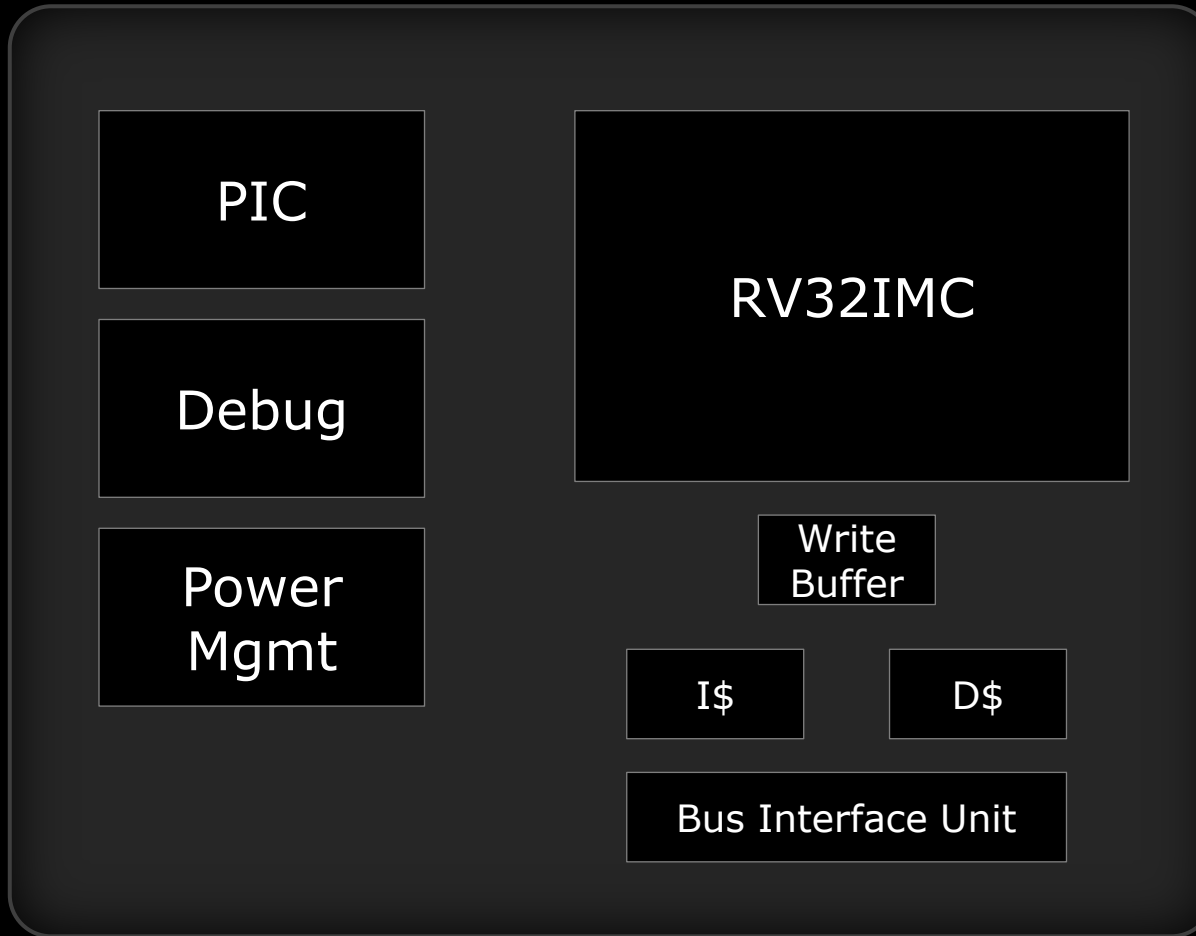
- First Western Digital RISC-V core
- 2-way, superscalar, mostly in-order core with 9 stages pipeline:
  - Support for RV32IMC
  - 1 Load/Store pipe
  - 1 MLY
  - 1 DIV
  - 4 ALU engines
- Performance targets @ 28nm:
  - Dhrystone >2 MIPS/MHz
  - Coremark > 3 CM/MHz
  - 1 GHz operation
- Core part was fun, uncore was all the work

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NAND Controller SoC
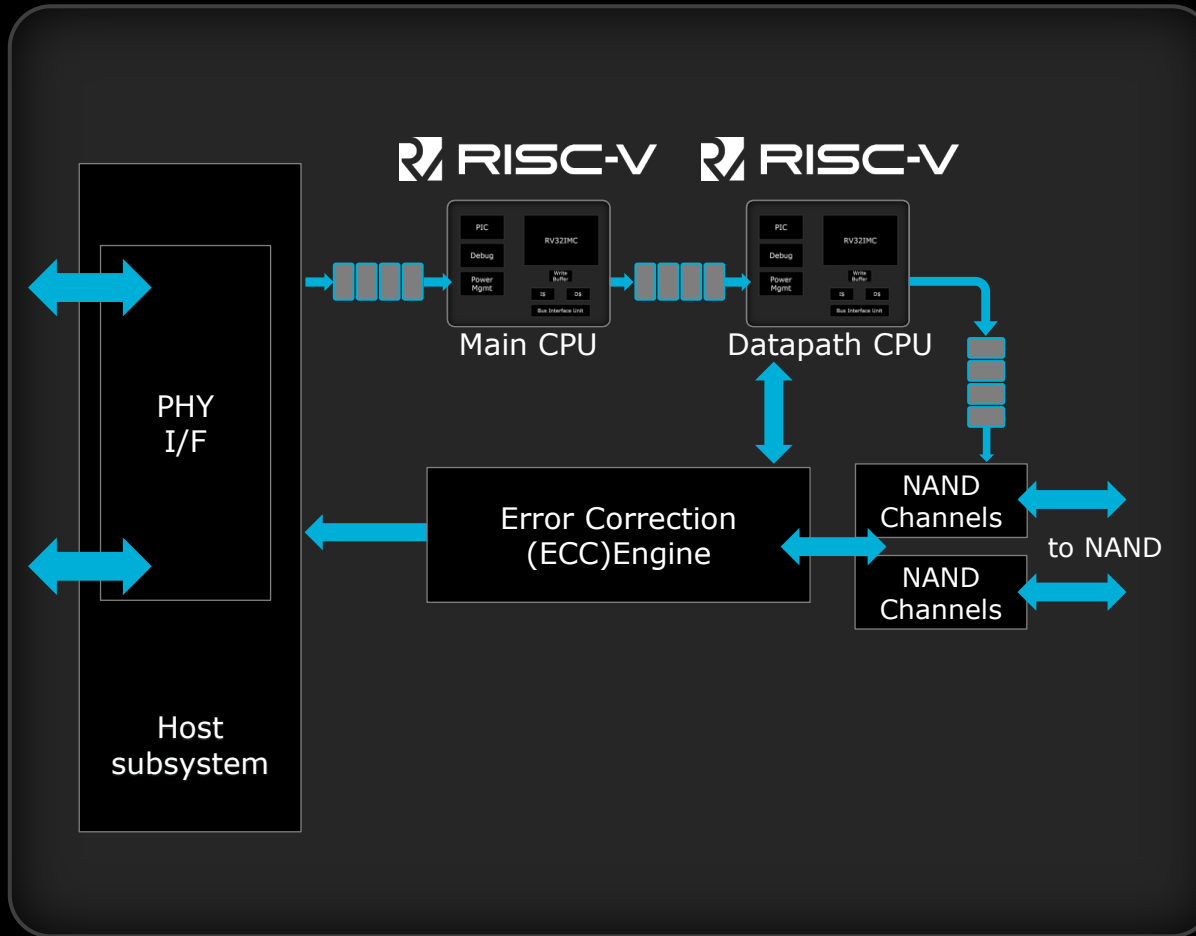
- Multi-purpose SoC for consumer SSD applications

- First RISC-V based SoC for NAND controller applications

- Advantages:
  - Full advantage of open source software ecosystem for RISC-V
  - Instruction optimization for NAND media handling
  - Freedom of power and performance optimization for end application

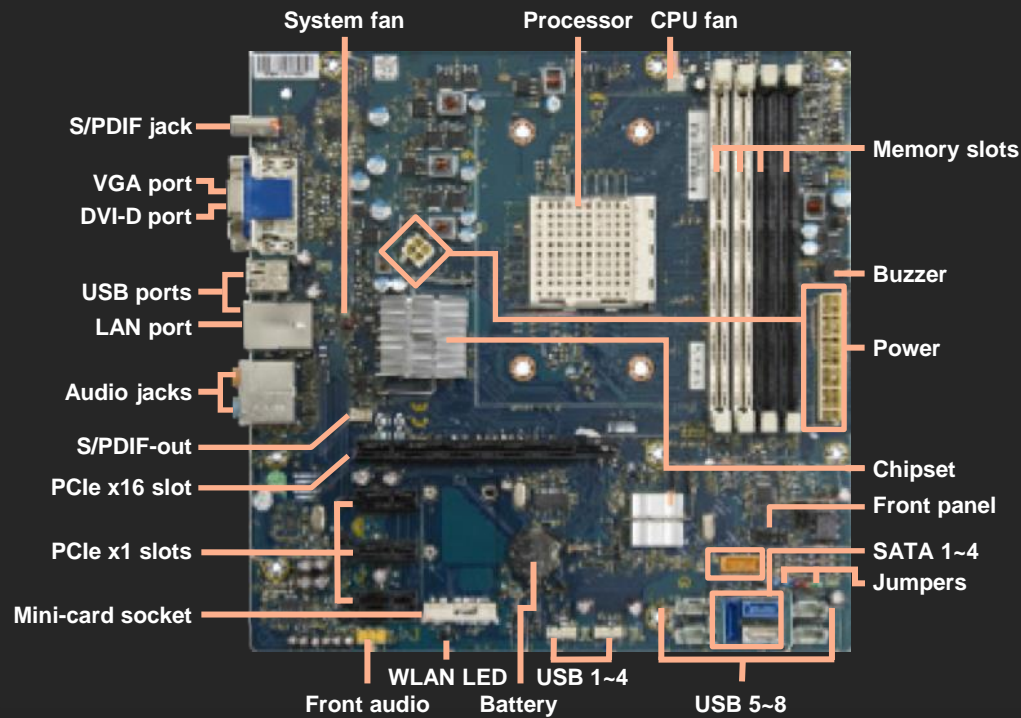# RISC-V and Interface Control Points
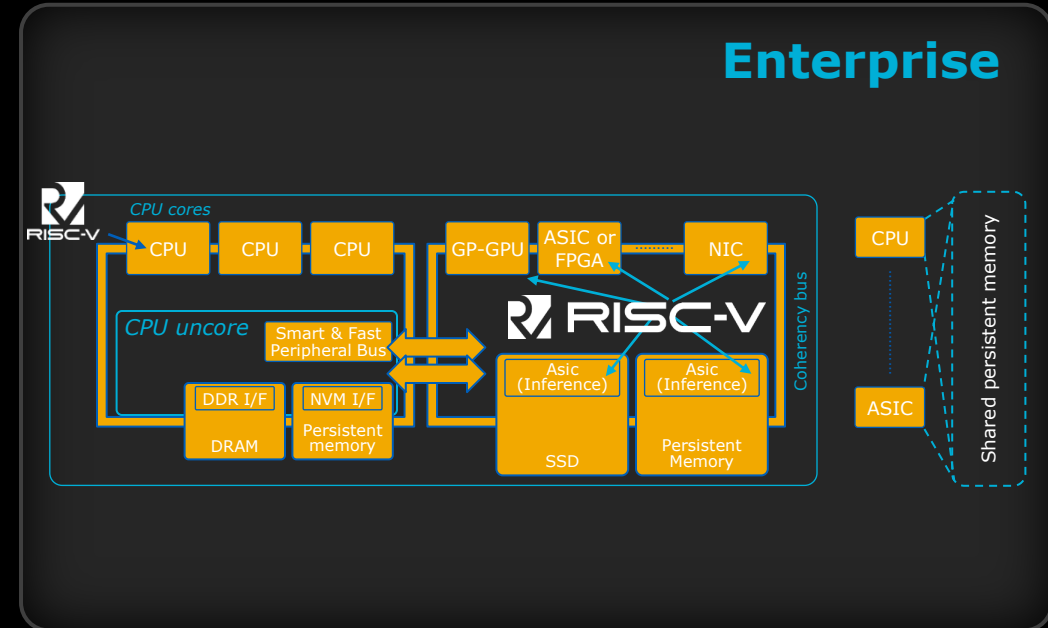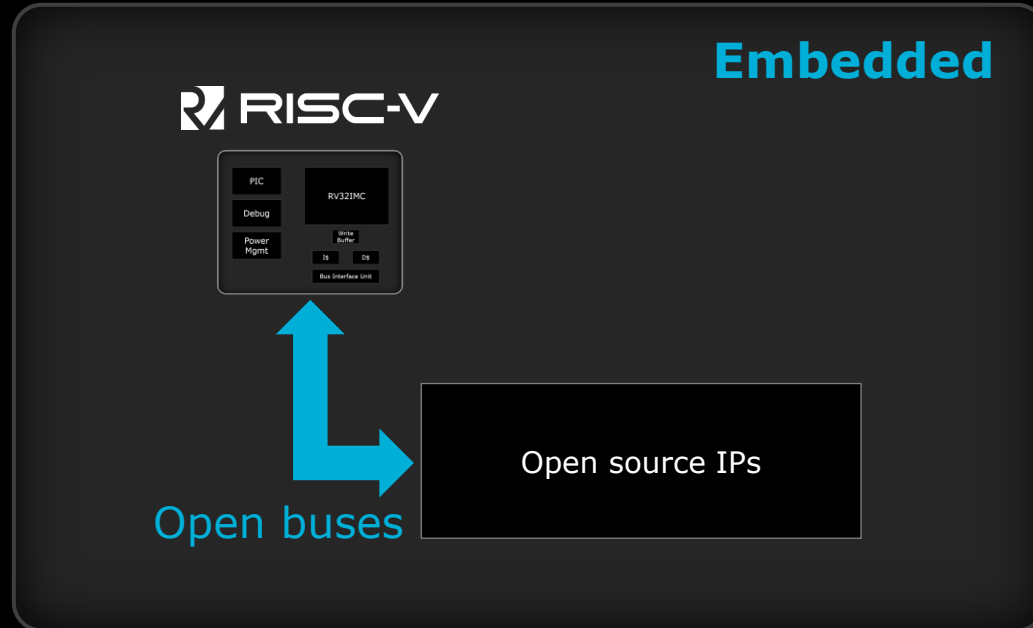
- RISC-V in embedded:
  - Free and open IP connectivity buses enabling plug and play of proprietary and open source IPs

- RISC-V in enterprise:
  - Datacenter CPUs with smart, fast and open peripherals buses enable new compute paradigms essential for AI workloads

General Purpose Architectures No Longer Sufficient

Big Data and Fast Data workloads exceed capability of uniform resource ratios

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General Purpose Transportation

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General Purpose Architectures No Longer Sufficient

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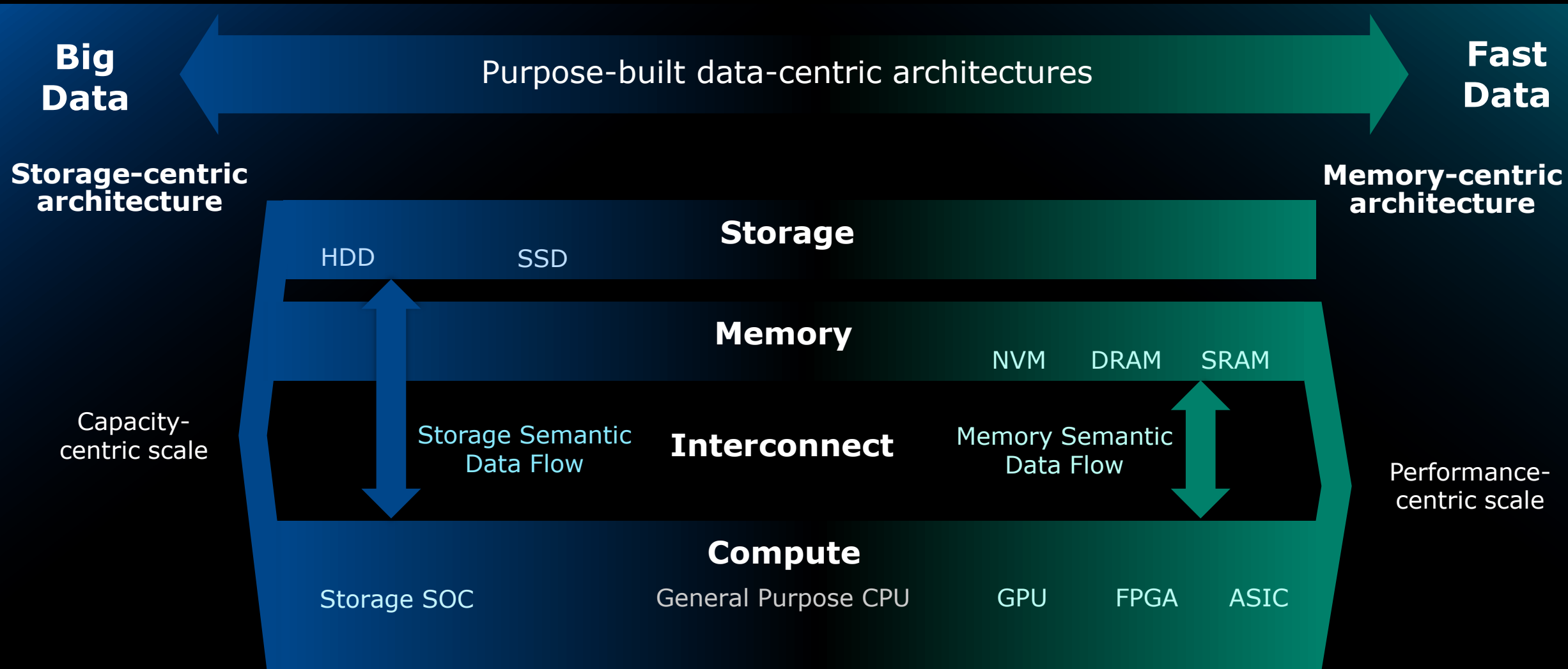
General Purpose Architectures No Longer Sufficient

Big Data and Fast Data workloads exceed capability of uniform resource ratios

Big Data

Fast Data

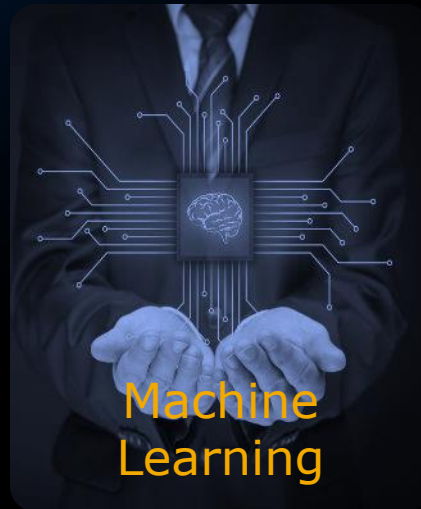# Workload Diversity Demands Diverse Technologies and Architectures

Big Data ← Purpose-built data-centric architectures → **Fast Data**

Storage-centric architecture

Memory-centric architecture

Storage

HDD   SSD

Memory

NVM   DRAM   SRAM

Capacity-centric scale

Interconnect

Storage Semantic Data Flow

Memory Semantic Data Flow

Performance-centric scale

Compute

Storage SOC   General Purpose CPU   GPU   FPGA   ASIC

Data-Centric Environments

Big Data and Fast Data workloads need independent scaling of resources

Big Data		Fast Data		
Analytics	Machine Learning	Security Detection	Event Correlation	Blockchain
• Massive Storage • Moderate Processing	• Massive Storage • Massive Specialty Processing	• Large Memory • Specialty Processing	• High-bandwidth interconnect • Large Memory and Specialty Processing	• High-bandwidth interconnect • Large Specialty Processing
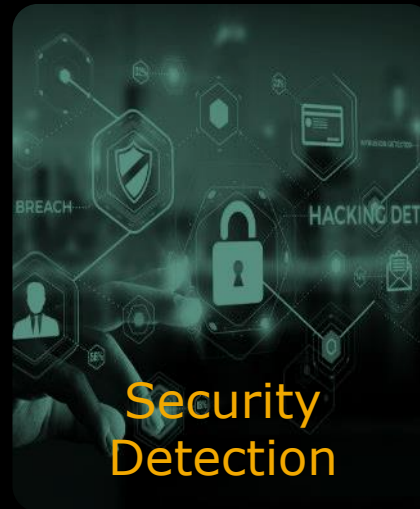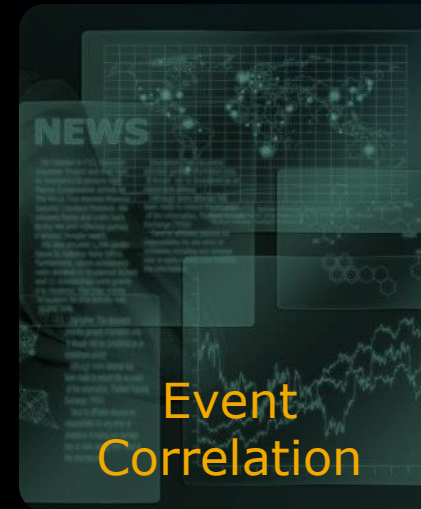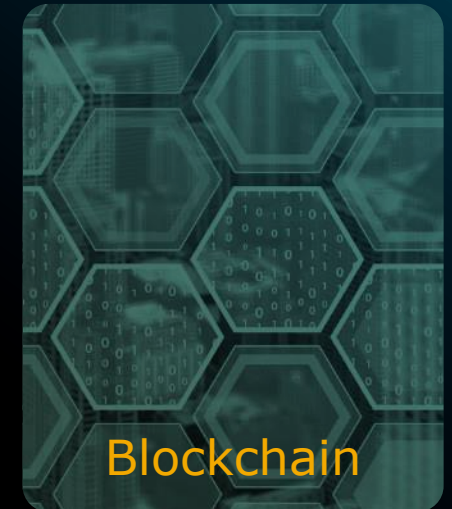
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Independent Scaling Demands Openness

Rapid adoption of new open source technologies and standards

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Data-Centric Applications at the Edge

Environments require modular technologies and dense integration to optimize space, weight and power consumption

RISC-V Meets the Needs of Big Data and Fast Data

Provides a foundation for purpose-built, data-centric compute environments

Big Data

Fast Data

Move Compute to Data

- CPU for device, platform, system
- Minimize data movement
- Offload workload to "smart" storage
- Localized machine learning

Memory Centric Compute

- Highly scalable main memory
- Minimize data movement
- Heterogeneous processor support
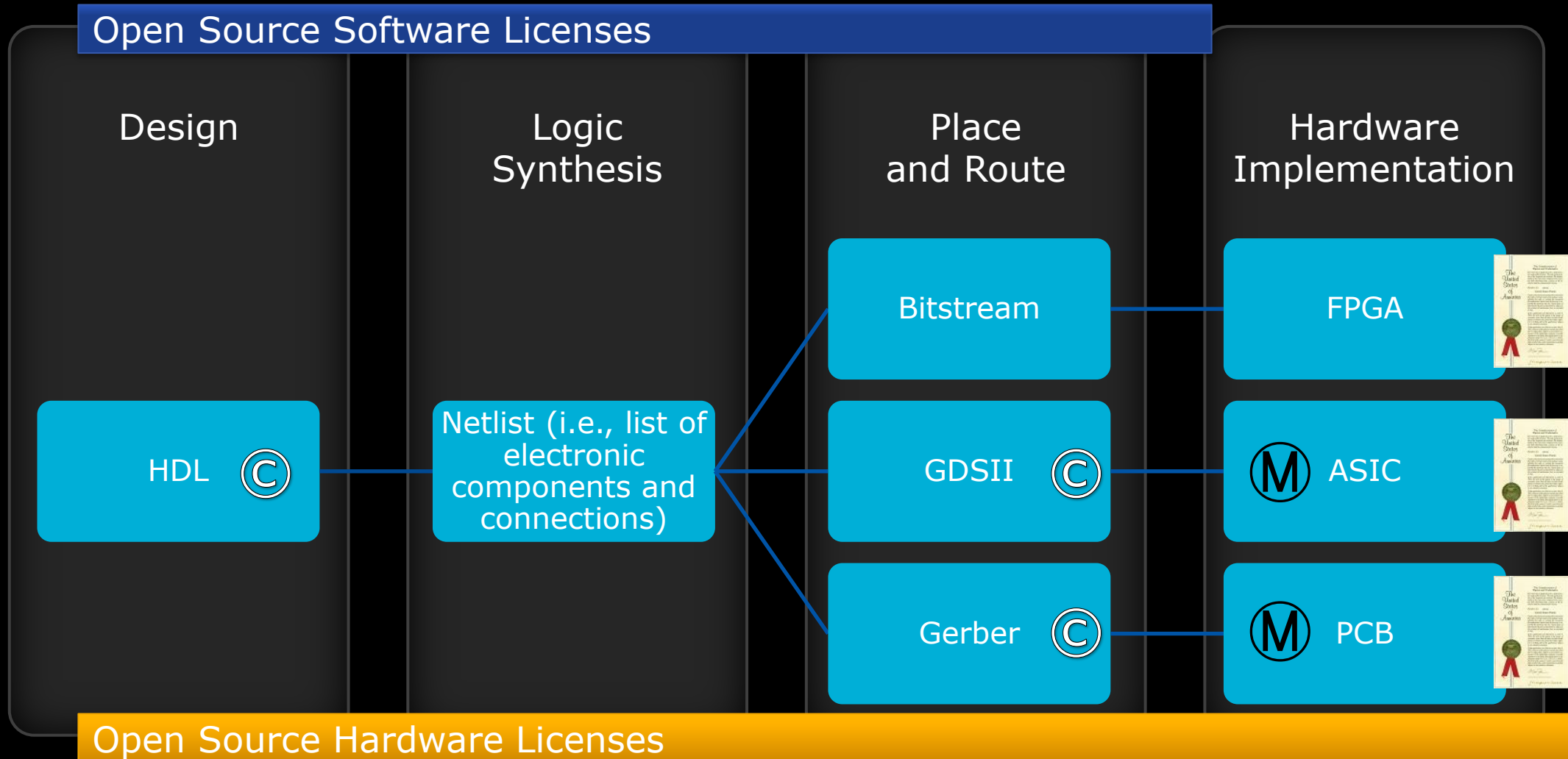- Scalable accelerators/offload engines

RISC-V

- Open and free
- Enables modular chip designs
- From 16 to 128-bit

- Scales from embedded to enterprise
- Direct integration with specialty accelerators
- Extensible ISA (for special purpose functions)

Permissive vs Copyleft

Licenses define the potential community

Permissive License

Goal:
Broad use of code

Copyleft License

Goal:
Reciprocity
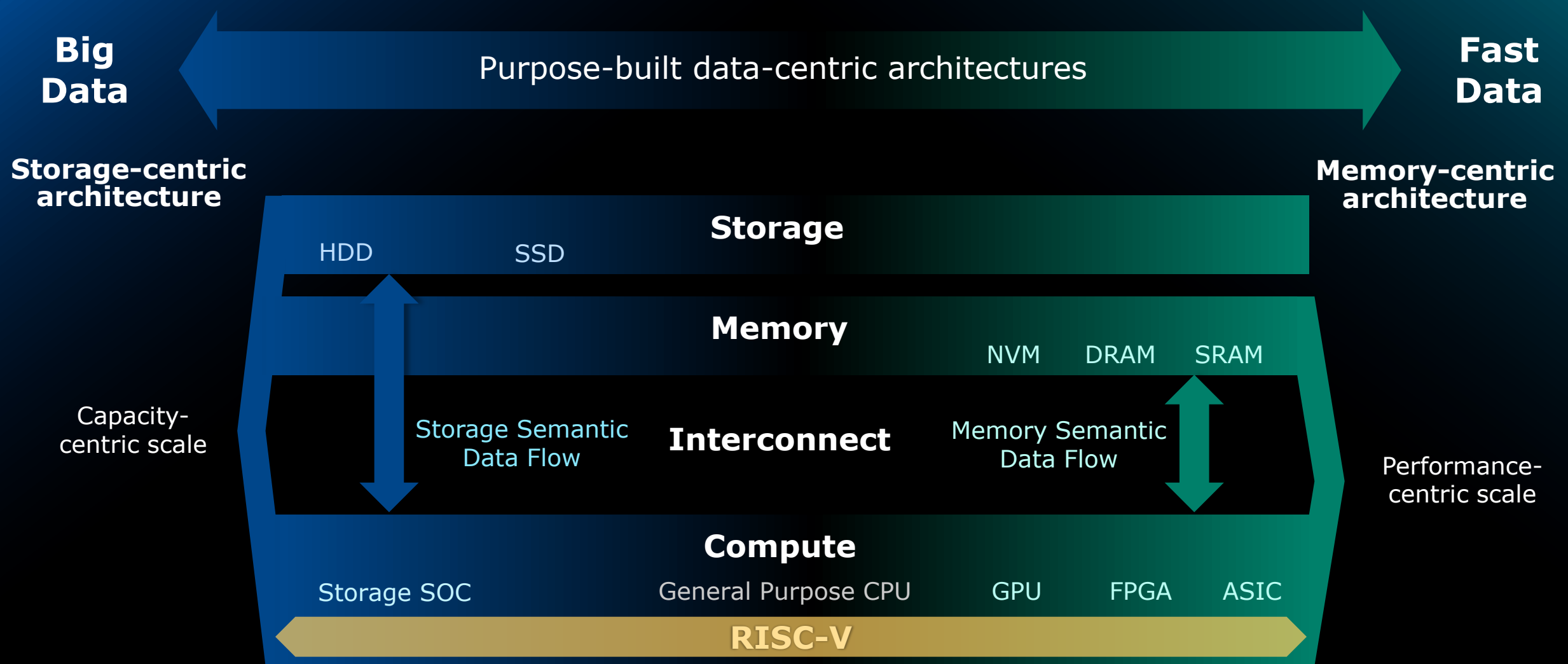
- Easier obligations
  - Attribution
  - More corporate adoption
- Allows for proprietary silos

- Harder obligations
  - Source code sharing
  - No DRM
  - Less corporate adoption
- Disallows proprietary silos
- May be incompatible with other components

RISC-V Enables Purpose-Built Environments for Big Data and Fast Data Applications

RISC-V Meets the Needs of Big Data and Fast Data

Big Data

Fast Data

Predictive Analytics

Autonomous Machines

Genomics

Safety & Security

Machine Learning

Private Exchange

RISC-V

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Driving Momentum

Western Digital ships in excess of
1 Billion cores per year
…and we expect to **double that**.

Accelerating the RISC-V Ecosystem

Western Digital to contribute one billion cores annually to fuel RISC-V

1 Support development of open source IP building blocks for the community

2 Actively partner and invest in the ecosystem

3 Accelerate development of purpose-built processors for a broad range of Big Data and Fast Data environments

4 Multi-year transition of Western Digital devices, platforms and systems to RISC-V purpose-built architectures

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Innovating for a Data-Centric World

Big Data and Fast Data need purpose-built environments

Openness and ecosystem enable best-in-class innovation

Western Digital brings the momentum of >1B cores per year

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