Agenda

- Introduction to TRACE32
- RISC-V Debug and Trace
  - Debug Scenarios
  - Custom ISA Extensions
  - Standardization
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► Introduction to TRACE32

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Introduction to TRACE32: Lauterbach

- Lauterbach: Leading manufacturer of microprocessor development tools
- Headquarters in Hoehenkirchen, Germany (nearby Munich)
- Branch offices in China (3), France, Italy, Japan, Tunisia, UK and USA (2)
- Approximately 120 employees worldwide
Introduction to TRACE32: Our Strengths

- Technical know-how at highest level
  - HW and SW debug and trace tools is all we do
  - All design, development and manufacture in Munich

- Run-control debugging via TRACE32
  - Debug and development of
    - (Bare-metal) applications
    - Operating systems
    - Drivers/Bios
    - Chip/board bring-up → debugging from the reset vector
Introduction to TRACE32: Our Strengths

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RISC-V Debug Scenarios

External Debugger: TRACE32

Debug Port & Interconnect

Standard Debug IP "External Debug Support v0.13"

RISC-V Core(s)

CHIP
RISC-V Debug Scenarios

External Debugger: TRACE32

Debug Port & Interconnect

Standard Debug IP "External Debug Support v0.13"

RISC-V Core(s)
RISC-V Debug Scenarios

- Support for a variety of external and internal interfaces
- Support for interconnections of standard debug specification v0.13: Debug Transport Modules (DTMs)
RISC-V Debug Scenarios

External Debugger: TRACE32

Debug Port & Interconnect

Standard Debug IP "External Debug Support v0.13"

RISC-V Core(s)

CHIP
RISC-V Debug Scenarios
RISC-V Debug Scenarios

- RISC-V multicore debugging:
  - Synchronous Multiprocessing (SMP)
    - Synchronization of reset, halt/resume, on-chip triggers, etc
  - Asynchronous Multiprocessing (AMP)
RISC-V Debug Scenarios

- TRACE32 Linux Awareness for RISC-V
  - Linux kernel 4.15 brings support for RISC-V
RISC-V Debug Scenarios

- TRACE32 Linux Awareness for RISC-V
  - Linux kernel 4.15 brings support for RISC-V
  - Debug processes, threads, dynamic objects (libraries and kernel modules)
  - View Linux resources:
    - task and kernel module list
    - addresses of dynamic objects
RISC-V Debug Scenarios

- Heterogeneous systems: debug different RV32, RV64 variants and cores of various other core architectures in one session
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Custom ISA Extensions

default extensions | custom extensions

M: Multiplication | X: custom #1
A: Atomic | X: custom #2
C: Compressed
Custom ISA Extensions

- Customer asks “do you support custom RISC-V extensions?” → what does “support” mean/affect?

- Different integration methods:
  - Direct integration in TRACE32 software
  - “APU” API
Custom ISA Extensions

- Direct integration in TRACE32 software
Custom ISA Extensions: APU API

- Integration via “APU” (Auxiliary Processing Unit) API

- Plugin provided as .dll/.so runtime library

- (Dis)assembler for custom instructions provided by user

- (Optional) integration of 3rd party software (e.g. own disassembler)
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Standardization of RISC-V Debug and Trace

- Fragmentation of Debug Ecosystem

**Diagram:**
- **External Debugger:** TRACE32
- **Debug Driver**
- **Standard Debug IP:** "External Debug Support v0.13"
- **RISC-V Core(s)**
  - **Debug Mode**
Standardization of RISC-V Debug and Trace

- Fragmentation of Debug Ecosystem
Standardization of RISC-V Debug and Trace

- Fragmentation of Debug Ecosystem
Standardization of RISC-V Debug and Trace

- Fragmentation of Debug Ecosystem

- Result:
  - More development cost and time for custom solutions
  - Fragmentation (unlikely that companies will change an established debug IP to standard afterwards)
  - Weakened RISC-V ecosystem
Thank you!

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