Designing a Commercial Libre RISC-V SoC

Ethical Strategic Leveraging of the benefits of Libre and Open SW/HW for pure unadulterated Commercial gain

Chennai 9th RISC-V Workshop

July 15, 2018
Credits and Acknowledgements

- The Designers of RISC-V
- The RISC-V Foundation
- The Shakti Group, and IIT Madras RISE Group
- Prof. G S Madhusudan
- Neel Gala
- Rishabh Jain
- Members of the RISC-V Open Groups (SW/HW/ISA)
- Libre and Open Software and Hardware Communities
- Richard Herveille (RoaLogic), Edmund Humenberger, Clifford Wolf (Symbiotica EDA), Rudi (Asics.ws), Enjoy-Digital.fr, Alex Forenchich, LowRISC Team
- Anonymous Sponsor
Why, How, What?

▸ Why? Because these days it’s just not necessary to make [un]ethical compromises in order to make a profitable, desirable mass-volume product

(There’s enough companies doing that: where it’s got us??)

▸ How? By leveraging the long-established strategic cost and maintenance benefits of libre-licensed software (and HDL) and making sure that the people who provide it are financially rewarded. Also by empowering diverse team collaboration

▸ What? A 2.5ghz RISC-V 64-bit SoC that has a 3D Embedded GPU, 1080p Video decode, and interfaces to make it attractive for use in tablets, netbooks, industrial embedded and more. 22nm or less, under 400 pins, under USD $4.

All sounds obvious... but is it practical and achievable?
Definitions

- **Business**: the provision of a service and being commensurately financially rewarded for doing so

- **Spongeing**: the provision of a service and being taken advantage of for doing so *(cf: Professor Yunus)*

- **An ethical act**: an act that increases truth, love, awareness or creativity for one or more people (including yourself), *without* reducing those same four qualities *for anyone*

- **The Four Freedoms**: the rights and guarantees associated with and embedded within GNU Licenses *(cf: FSF)*

*Is it possible to ethically do business and respect the Four Freedoms? That’s where it gets interesting, as there are even cases where the Four Freedoms are unethical. Note: google’s former motto ”don’t be evil” is clearly (unintentionally) unethical*
Does what we want already exist? Surely this is nonsense!

Analysis of SoCs over the past 7+ years (answer: no)
Breakdown of non-existence of fully-Libre SoCs

- **iMX6**: Libre bootable, Vivante 3D GPU (libre etnaviv) but proprietary VPU (and a power-hungry Cortex A9)
- **Allwinner SoCs**: mostly Libre bootable, VPU reverse engineered; GPU: MALI or PowerVR (i.e. proprietary)
- **Rockchip SoCs**: good but using MALI or PowerVR.
- **TI OMAP**: good but using PowerVR. and expensive.
- **Samsung**: good but using MALI.
- **Ingenic jz4775**: GREAT! performance sucks (1ghz MIPS32).
- **Broadcom SoCs**: Cartelled. and boots from the GPU

Basically there does not exist one single commercial SoC that provides full source code for all functions (CPU, GPU, VPU) with modern performance. Which is kinda bizarre if you think about it.
What would a good (Libre) boring, mundane SoC have?

- Cover a lot of different scenarios (embedded, tablets, industrial, netbooks, crypto-currency mining).
- Decent performance with high efficiency. RISC-V: 40% more efficient than ARM / Intel. Shakti a good candidate: 2.5ghz and 120mW per core @ 22nm.
- 1080p video: y’all gotta watch cute kittens on youtube, right?
- 3D GPU: y’all gotta play Angri Burds, right? (or Minecraft)
- No spying back-door co-processors (to steal crypto-wallets)
- No Spectres, no Meltdowns.

Basically quite boring and mundane. No Monster Performance, no AI stuff, no special sauce. Just a plain-old SoC, 40% more power efficient than ARM/Intel, and not spying on end-users, that’s all.
How on earth does an ethical Libre SoC make money???

- Simple answer: Mask Rights.
- Without Mask Rights: by having a desirable product, and packaging it for a customer (i.e. by being a middle-man a service is still being provided for which payment etc. etc.)
- Without a desirable product or customer(s): err... you don’t. (cf: definition of Business)
- By not having high NREs (leveraging back-to-back deals, and helping others fulfil their needs and goals)

*Detachment from the goal also helps. If someone else makes this product then GREAT! I can go do something else*

Main point: please do not automatically assume Ethical and Libre is non-commercial. It’s not nice, and it’s not helping
Things wot are ”off-limits”

- Customer entrapment (through proprietary software). Strong business case for not entrapping customers: https://tinyurl.com/most-productive-meeting-ever
- Funding, endorsing, supporting or empowering unethical Companies, Organisations, Cartels and Individuals. (cf: definition of an ethical act).
- Being totally inflexible / unrealistic. Goals have to be met: it’s no good being an idiot about that. e.g. if a Libre 3D GPU really can’t be made, use Vivante GC800 (with etnaviv).
- Spying back-door co-processors a no-no. Sovereignty is critical. Russia has Baikal. China has Loongson.

*Still no real show-stoppers to making money (or product): it’s just slightly harder, that’s all. Ultimately it’s about confidence.*
Separate Power Domains for GPIO banks, Variable voltages required, low-power sleep states etc. Quite involved
Hardware / Development Complexity Comparison

- **Server**: relatively easy. PCIe, RapidIO, XAUI, SATA, GbE, 10GE, DDR3/4 (or HMC) etc. etc. No multiplexing: all interfaces dedicated and high-speed differential pairs.

- **Desktop**: really just a variant of Server. Graphics is a PCIe Card (except if integrated). Peripherals often done in dedicated external ICs ("Southbridge" concept)

- **Embedded**: also pretty easy. Really needs a pinmux. Low clock rate, low power mode. e.g. SiFive Freedom U310.


*Bottom line: Mobile-class processors are challenging!*
Proprietary vs Libre-licensed Interface HDL

- DDR3/4: challenging! $1m for single-use, single instance. Symbiotic EDA: $600k for PHY; CERN developed a Controller
  http://libre-riscv.org/shakti/m_class/DDR/
- HyperRAM (JEDEC xSPI): lower risk than DDR3/4
  http://libre-riscv.org/shakti/m_class/HyperRAM/
- RGMII: several available (saves $50k)
  http://libre-riscv.org/shakti/m_class/RGMII/
- UART, SPI, I2C, PWM, SD/MMC: all libre (except eMMC).
- Shakti Group has FlexBus, QuadSPI, SRAM, many more.
- RGB/TTL: R. Herveille (SSD2828, SN75LVDS83b, TFP410a)

Basically there’s no compelling reason to spend vast sums on proprietary HDL. Sorry Cadence / Mentor / Synopsis / whoever
DDR3/4 PHYs are analog and very high speed. Impedance training. Extreme timing tolerances on parallel buses. No surprise proprietary cost is USD $1m and above.

Symbiotic EDA will do (Libre) PHY layout for USD $300k, time to completion for chosen geometry: 8-12 months.

Silicon-proven but still risky. What are the alternatives?

- FlexBus/SDRAM (low clock, lots of pins, single-data-rate).
- HyperRAM (aka JEDEC xSPI) 8-bit SPI 166mhz or DDR-300. 300mbyte/sec for only 13 wires, not bad! (We’ll take several) http://libre-riscv.org/shakti/m_class/HyperRAM/
- HMC: insanely fast, very low power. OpenHMC (LGPL) https://opencores.org/project/openhmc
Richard Herveille’s Video Core Blocks
https://opencores.org/project/video_systems

Symbiotic EDA MP4 decoder in FPGA

H.264 seems to have been done...
https://github.com/adsc-hls/synthesizable_h264

Really needs SIMD (or better, not-SIMD)
http://libre-riscv.org/simple_v_extension/

Definitely needs xBitManip (parallelised by Simple-V)
https://github.com/cliffordwolf/xbitmanip

**SIMD is insane.** \(O(N^6)\) opcode proliferation. See
https://www.sigarch.org/simd-instructions-considered-harmful/

(1): P-Ext designed for Audio. (2): Investigate RI5CY’s SIMD

- Been done before (many times), but not as a Libre Design.
- Sanjay Charagulla: GlobalFoundries 22nm mobile process can reach as low as 0.4v
- GPIO Banks need per-bank VREF (1.8v? to 3.3v)
  IO pads need built-in level-shifting to convert to CPU VCORE
- Each core needs independent variable-voltage capability and independent shut-down (PMIC supplies external voltage)
- DDR RAM still needs refreshing (even in sleep mode)
- Extra RV32 (PicoRV32?) always-on core for wake-up / RTC
- PLLs are Analog. fun fun fun fun in the sun sun sun sun...

Really need help. PLLs, Analog stuff: specific domain expertise.
Fall-back example: https://www.dolphin-integration.com?

- Actual requirements quite modest: 30MP/s 100MT/s 5GFLOPS but power/area is crucial (2mm² @ 40nm, 1W)
- Nyuzi, MIAOW, GPLGPU (Number Nine), OGP.
- Nyuzi based on Larrabee. Jeff Bush really helpful.
- MIAOW is an OpenCL engine. GPLGPU is fixed-function
- Nyuzi lessons: Software-only rendering not enough. Getting through L1 cache takes most power. Fixed functions such as parallel FP-Quad to ARGB Pixel, and Z-Buffer needed.
- Fallback is GC800 ($250k) contact me if you can do better!

Jacob Bachmeyer’s Cache-control proposal turns L1 Cache into scratchpad RAM. RVV is just too heavy (sorry!), Simple-V much more light-weight and flexible (O(1) ISA proliferation)
GPUs are usually done with incompatible ISAs and effectively doing OpenGL over IPC / RPC (Remote Procedure Calls).

Much simpler: GPGPU “one ISA” approach. Custom-extend the core ISA to handle 3D, use Gallium3D-LLVM.

Now add Video Extensions. and SIMD etc and we are well beyond the only 2 available 32-bit custom opcodes.

Due to the Libre nature of this project, the custom opcode space will be ”dominated” by high-profile public hard-forks of gcc, binutils, llvm etc. Which isn’t going to go down well.

ISA ”Conflict Resolution” is therefore absolutely critical.

http://libre-riscv.org/isa_conflict_resolution/

Remember Altivec. Learn from Intel. This is everyone’s problem.
Interesting Missing Stuff [1] - Pinmux

- Pinmux: multiplexer of functions onto pins
  \[ \text{DRAM Cell } \neq \text{DDR3/4, Mux Cell } \neq \text{Muxer} \]

- Strategically extremely important to Commercial SoC success
  STMicro, Rockchip, Freescale, Samsung, TI, \textbf{EVERYONE}

- Bizarrely, a libre-licensed multi-way Pinmux doesn’t exist.
  \textit{not on anyone’s radar. at all. SiFive IOF not enough.}

- Verification (scenario analysis) and auto-generation of TRM,
  header files, device-tree files, pretty much everything makes
  sense (to any ”lazy” Software Engineer...)

- Corporations with legacy pinmux unlikely to be interested.

- \texttt{http://git.libre-riscv.org/?p=pinmux.git}
  \texttt{http://hands.com/~lkcl/pinmux_chennai_2018.pdf}
Interesting Missing Stuff [2] - AC97/I2S, USB2 PHY

▶ Rudi (Asics.ws) donating time to create a Multi-Protocol Audio Controller: AC97, PCM, PDM, I2S
   http://libre-riscv.org/shakti/m_class/AC97/

▶ USB2 is... convoluted. UTMI-ULPI-USB2 PHY
   USB2-PHY not confirmed (Rudi has one)
   Also Rudi has DDR (8-pin) variant of ULPI
   http://libre-riscv.org/shakti/m_class/ULPI/

▶ USB3 not necessarily a good idea to put into Libre-RISCV
   Daisho USB3 Pipe exists, TUSB1310a PHY is 175 pin FBGA!

▶ Libre SD/MMC typically at "Open" Level 20MB/sec appx.
   Full spec and eMMC needed (Rudi again).

Trying to keep interfaces all-digital (USB3 isn’t, HP/Mic definitely isn’t). Use external (Analog) PHYs and/or Multi-chip Module
Which Processor Cores to use?

- Shakti RV64 at the top of the list, not just for technical reasons, but for the Shakti Group’s goals and vision.

- Libre 3D GPGPU (SMP RV64 plus accelerated custom ISA) would make things interesting (3D app pinned to a non-uniform but SMP architecture)

- Video Processing again is reasonable to be a different RV32/64 Core (SMP or otherwise), possibly not even RV at all (MIPS, OR1200)

- RV32 (PicoRV32?) always-on definitely needed (sleep mode)

*Ultimately, decisions are flexible, heavily weighted towards ”what does good and doesn’t do bad” as well as cost vs risk*
Making a commercially-desirable SoC is neither academically nor standard-investor sexy! No AI. Boring. zzzz

Luckily there is an anonymous sponsor who needs an SoC that doesn’t exist (who knows the commercial benefits of Libre)

Shakti Group know the benefits (cost, sovereignty) of a Libre Mobile-Class SoC as well (No spying on India citizens!)

A Libre GPU, even a modest performer (100MT/s etc.) is the biggest technical risk/unknown, besides DDR3/4. (fall-back is GC800. Do please help with a Libre GPU!)

DDR3/4 and eMMC are the main high-risk interfaces (there are fall-back strategies in place)

Ultimately the strategy is all about cost reduction vs risk mitigation, with Libre/Ethical prioritised over "convenience"
The end
Thank you
Questions?

- Contact: lkcl@lkcl.net
- http://libre-riscv.org/shakti/m_class/