RVS – RISC-V Verification Suite for Architectural Compliance and Functional Testing

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RISC-V Verification Suite for Architectural Compliance and Functional Testing

Collection of a large number of tests based on STING’s design verification framework

Tests are based on scenarios identified in verification plan developed by Valtrix

Stimulus is a mix of constrained random, control graph based, directed, C++ based test generation mechanisms

Portable across all DUT environments i.e. RTL, emulation, FPGA and silicon

Proprietary stimulus generation mechanisms allows for higher cross product coverage for tests

STING kernel’s execution framework allows easy integration into a SoC like environment

Verification packages can be easily created depending on the needs of the target implementation

All tests are architecturally correct and reference model verified

Enabled on simulations of Rocket, PULPino, Ariane along with SPIKE and QEMU simulators

Completely supports RV32 and RV64 base integer instruction sets and extensions defined in user level specification; Certain sections of floating point is WIP

Supports multi processor (MP) test execution in user, supervisor and machine privilege levels; All CSRs, virtual memory systems covered

Regression and coverage collaterals around the verification suite present

Ample amount of debug information available with all the tests to debug the failures coming out of execution