RISC-V: Enabling Innovation in Embedded and Enterprise Data-Centric Computing Architectures

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Diverse and Connected Data Types

Tight coupling between Big Data and Fast Data

Big Data
- Insight
- Prediction
- Prescription
- Scale

Fast Data
- Mobility
- Real-time Results
- Smart Machines
- Performance

Data Aggregation
Batch Analytics
Modeling
Artificial Intelligence
Machine Learning
Streaming Analytics

ALGORITHMS
DATA

Insight
Prediction
Prescription
Scale
From General Purpose to Purpose Built

Architectures designed for Big Data, Fast Data applications

General purpose compute-centric architecture

Solutions
Systems
Platforms
Devices
What’s Different about RISC-V?

• **Simple**
  – Far smaller than other commercial ISAs

• **Clean-slate design**
  – Clear separation between user and privileged ISA
  – Avoids µarchitecture or technology-dependent features

• A **modular ISA designed for extensibility/specialization**
  – Small standard base ISA, with multiple standard extensions
  – Sparse and variable-length instruction encoding for vast opcode space

• **Stable**
  – Base and standard extensions are frozen
  – Additions via optional extensions, not new versions

• **Community designed**
  – Developed with leading industry/academic experts and software developers
RISC-V for IoT/Embedded

• IoT key requirements:
  – Performance:
    • Tuned for the applications, typically by moving SW/HW boundary and adding custom accelerator appropriate for the workload
  – Power:
    • Scalable architecture for performance vs. power compromise
    • Some IoT applications may require implementation area <0.05 mm^2 and few mW
  – Freedom to implement custom accelerators for specific workload
RISC-V for IoT/Embedded

• Challenges with closed architectures:
  – Fixed set of cores offered to customers:
    • Does not cover all power/performance scenarios; often has unnecessary IP (do you really need double precision IEEE754 FPU in the refrigerator IoT device)
  – Does not cover all accelerators needed:
    • Leakage of use cases and solutions to IP vendors
  – Not having right accelerators for all markets – rapidly evolving use cases
Western Digital: Key Requirements

• Key requirements:
  ✓ Improve performance
  ✓ Reduce power
  ✓ Enable tightly coupled memories
  ✓ Open source software support
  ✓ Implement internal system bus
  ✓ Enable adding proprietary and future standard instructions

Not all cores will be in-house – some may be open-source, some internal will be open-source, some may be licensed:
   but all with adhere to the same RISC-V specification, guaranteeing COMMON Software ToolChain!
Western Digital RISC-V Core

• First Western Digital RISC-V core
• 2-way, superscalar, mostly in-order core with 9 stages pipeline:
  – Support for RV32IMC
  – 1 Load/Store pipe
  – 1 MLY
  – 1 DIV
  – 4 ALU engines
• Performance targets @ 28nm:
  – Dhrystone >2 MIPS/MHz
  – Coremark > 4 CM/MHz
  – 1 GHz operation
• Core part was fun, uncore was all the work
• WD Core is currently at 4.9 CoreMark/MHz, ahead of all RISC-V cores, including many industry and academia out of order implementations:
  – Additional performance gains are possible with compiler optimizations
  – Multi-threaded/multi-core results are always renormalized to a single execution context

CoreMark data from C.Celio, D.Patterson, K.Asanovic,https://www2.eecs.berkeley.edu/Pubs/TechRpts/2015/EECS-2015-167.pdf
NAND Controller SoC

• Multi-purpose SoC for consumer SSD applications
• First RISC-V based SoC for NAND controller applications
• Advantages:
  – Full advantage of open source software ecosystem for RISC-V
  – Instruction optimization for NAND media handling
  – Freedom of power and performance optimization for end application
RISC-V and Interface Control Points

*Embedded*

- RISC-V in embedded:
  - Free and open IP connectivity buses enabling plug and play of proprietary and open source IPs

*Enterprise*

- RISC-V in enterprise:
  - Datacenter CPUs with smart, fast and open peripherals buses enable new compute paradigms essential for AI workloads
Hardware Design Lifecycle

Legal protections with copyrights, mask works and patents

Open Source Software Licenses

Design
- HDL

Logic Synthesis
- Netlist (i.e., list of electronic components and connections)

Place and Route
- Bitstream
- GDSII
- Gerber

Hardware Implementation
- FPGA
- ASIC
- PCB

Open Source Hardware Licenses
Permissive vs Copyleft

Permissive License

Goal: Broad use of code

- Easier obligations
  - Attribution
  - More corporate adoption
- Allows for proprietary silos

Copyleft License

Goal: Reciprocity

- Harder obligations
  - Source code sharing
  - No DRM
- Less corporate adoption
- Disallows proprietary silos
- May be incompatible with other components
RISC-V Meets Big Data and Fast Data Needs

Big Data
- Predictive Analytics
- Genomics

Fast Data
- Autonomous Machines
- Safety & Security
- Private Exchange
- Machine Learning

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#LetDataThrive
Western Digital ships in excess of **1 Billion** cores per year
...and we expect to **double that**.
Accelerating the RISC-V Ecosystem

Western Digital to contribute one billion cores annually to fuel RISC-V

1. Support development of open source IP building blocks for the community

2. Actively partner and invest in the ecosystem

3. Accelerate development of purpose-built processors for a broad range of Big Data and Fast Data environments

4. Multi-year transition of Western Digital devices, platforms and systems to RISC-V purpose-built architectures
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