Mi-V RISC-V Ecosystem
Agenda

- RISC-V Primer
- Mi-V Ecosystem
  - RISC-V Soft Processor Offerings
  - Tools
  - Debug
  - Benchmarks
  - Kits
- Mi-V Ecosystem for Linux
  - Unleashed Expansion
  - Demo Machine Learning
- Summary
What is RISC-V?

- A new, free, and open ISA developed at UC Berkeley
  - Using a permissible BSD license

- ISA is designed for
  - Simplicity: <50 instructions required to run Linux
  - Longevity: standardized instructions are fixed—your code runs forever

- RISC-V foundation set up to
  - Protect the ISA
  - Foster adoption

- RISC-V is not an open-source processor
  - Although open-source implementations will exist
  - Provides everyone an “architectural” license to innovate
RISC-V Working Groups/Chairs

- Base ISA Ratification—Berkeley
- Bit Manipulation—AMD
- Compliance—Microsemi/Codasip
- Debug—SiFive
- Formal Spec—Bluespec
- Memory Model—NVIDIA, MIT
- Opcode Space Management—Berkeley
- Privilege Spec—SiFive
- SW Tool Chain—BAE
- Vector Extensions—Berkeley, Esperanto Technologies
- Security—Nvidia

*Bold = Microsemi Participation*
Why RISC-V for Soft CPUs?

- Open-source ISA
  - Freedom to innovate at the micro-architectural level
  - Allows for RTL inspection—trust and certifications
  - Backed by industry leaders

- Longevity
  - Fixed ISA for long-term code portability
  - Easy migration to an ASIC
    - Without negotiating a license from ARM

- Proprietary/closed alternatives
  - ARM® Cortex-M1—encrypted RTL
  - NIOS (Intel) and MicroBlaze (Xilinx), licensed

*Open. Lowest Power. Programmable RISC-V Solutions.*
## Current SoC FPGA Offering

<table>
<thead>
<tr>
<th>Features</th>
<th>SmartFusion ProASIC3, IGLOO</th>
<th>SmartFusion2 IGLOO2</th>
<th>PolarFire</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Elements</td>
<td>100–30K</td>
<td>5K–150K</td>
<td>100K–480K</td>
</tr>
<tr>
<td>Transceiver Rate</td>
<td>1 Gbps–5 Gbps</td>
<td></td>
<td>250 Mbps–12.7 Gbps</td>
</tr>
<tr>
<td>I/O Speeds</td>
<td>400 Mbps LVDS</td>
<td>667 Mbps DDR3</td>
<td>1600 Mbps DDR4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>750 Mbps LVDS</td>
<td>1.6 Gbps LVDS</td>
</tr>
<tr>
<td>DSP (18x18 Multipliers)</td>
<td></td>
<td>240</td>
<td>1480</td>
</tr>
<tr>
<td>Max RAM</td>
<td>144 KB</td>
<td>5 MB</td>
<td>33 MB</td>
</tr>
<tr>
<td>Processor Option</td>
<td>100 MHz ARM Cortex-M3</td>
<td>166 MHz ARM Cortex-M3</td>
<td>Soft RISC-V Crypto Co-Processor</td>
</tr>
<tr>
<td>On-Board Flash</td>
<td>Up to 512 KB code store</td>
<td>Up to 512 KB code store</td>
<td>56 KB secure NVM</td>
</tr>
<tr>
<td>Family Type</td>
<td>CPLD replacements</td>
<td>Low-density FPGAs with more resources and the lowest power</td>
<td>Mid-range density FPGAs Lowest power, cost optimized</td>
</tr>
</tbody>
</table>

**Hard Processor Subsystems, Soft RISC-V CPUs**
Mi-V Ecosystem for PolarFire, RTG4, and IGLOO2 FPGAs

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Mi-V Ecosystem Components

A Comprehensive Ecosystem to Support RISC-V Development
### CPUs: Mi-V Soft CPU Roadmap

<table>
<thead>
<tr>
<th>Core</th>
<th>LEs</th>
<th>CoreMark</th>
<th>Cache</th>
<th>Mul/Div</th>
<th>Floating Point</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>CORE_RISCV_AXI4</td>
<td>10K</td>
<td>2.01</td>
<td>8K I and D</td>
<td>Yes</td>
<td></td>
<td>Now</td>
</tr>
<tr>
<td>Mi_V_RV32IMAC_L1_AHB</td>
<td>10K</td>
<td>2.01</td>
<td>8K I and D</td>
<td>Yes</td>
<td></td>
<td>Now</td>
</tr>
<tr>
<td>Mi_V_RV32IMACF_L1_AHB</td>
<td>26K</td>
<td>2.01</td>
<td>8K I and D</td>
<td>Yes</td>
<td>Single Precision</td>
<td>Now</td>
</tr>
<tr>
<td>Mi_V_RV32IC_AHB</td>
<td>4K</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Q2’18</td>
</tr>
</tbody>
</table>

- **New** Single Precision Floating Point core being released now
- **Mi_V_RV32IC_AHB**
  - Small core, without debug, estimate 4K LEs
- Additional cores to be added based on customer demand

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Mi-V = Mi-V RISC-V ecosystem  
RV32I = 32-bit integer machine  
M = Multiply and divide  
A = Atomic instructions  
F = Single precision floating point  
D = Double precision floating point  
C = Compressed instructions  
L1 = Instruction and data cache  
AHB = AHB bus interface  
AXI = AXI bus interface
Mi-V RISC-V Soft CPU on PolarFire/RTG4/IGLOO2 FPGAs

- 5-stage pipeline
- 8K I/D cache
- Integer mul/div
- 2 breakpoints
- 31 interrupts
  - Priority by Int #
- 1.1 DMIPS/MHz
- 10K LEs
- 50 MHz–150 MHz
  - Depending on product
# Boot Sources for Mi-V RISC-V Soft CPUs

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Non-Volatile Source</th>
<th>Off-Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>On-Chip—Secure Boot (KB)</td>
<td></td>
</tr>
<tr>
<td>sNVM</td>
<td>uPROM</td>
<td>eNVM</td>
</tr>
<tr>
<td>PolarFire</td>
<td>56</td>
<td>37–64</td>
</tr>
<tr>
<td>RTG4</td>
<td></td>
<td>46</td>
</tr>
<tr>
<td>IGLOO2</td>
<td></td>
<td>128–512</td>
</tr>
</tbody>
</table>

sNVM: PUF-protected R/W NVM  
uPROM: Read-only NVM  
eNVM: R/W NVM

The Only FPGA Supplier with Secure Boot Built-In and Open, Inspectable CPUs
SoftConsole Eclipse IDE

- A single tool chain for RISC-V and ARM MCUs
  - Easy migration from ARM to RISC-V
- Running on Linux or Windows hosts
- Supported by a Tier 1 supplier
- Bundled with example projects and RTOSs
Firmware Catalog

- Drivers for Microsemi RISC-V soft CPUs
  - Updates pushed to your desktop
  - Release notes
  - User guides
- Version controlled
- MISRA/Netrino compliant
Software Debug

- Soft CPUs support 8 breakpoints
- GDB open OCD debug
- OpenOCD supports a wide range of dongles
  - FlashPro5
  - Olimex ARM-USB-TINY-H
Boards: Mi-V Platforms

- **Microsemi Soft CPUs on FPGAs**
  - PolarFire
  - RTG4
  - IGLOO2

- **SiFive Freedom Unleashed Platforms**
  - HiFive1 FE310 Arduino platform validated with SoftConsole
Solutions: Example Designs on Github

- Design examples targeted to various boards
  - Hello world printf through UART
  - Interrupt blinky
  - Touch screen tic-tac-toe
  - Crypto processor with RISC-V

- Getting started building a RISC-V tutorial

- RISC-V hardware abstraction layer to port from Cortex-M
Operating Systems: Mi-V RISC-V Soft CPU RTOS Support

- **Open Source**
  - FreeRTOS
  - Huawei LiteOS
  - MyNewt
  - Zephr (Hifive)

- **Commercial**
  - ExpressLogic—ThreadX
  - SiLabs—Micrium μC/OSIII

MicroPython
Mi-V Supporting Linux
Mi-V HiFive Unleashed Expansion: Advancing the Ecosystem

- Enables the community to port tools, OS’s, middleware, packages to RISC-V
- Makes software development easier
- Enables standard and custom peripherals

- Supporting the community supports our soft CPUs for our FPGAs
- Supporting the community supports the MI-V ecosystem and vice versa
SiFive U-54 Block Diagram and Partnership

TSMC Shuttle Run October
PolarFire HiFive Unleashed Development Platform

- Designed for Expandability
- Pre-programmed with a ChipLink to PCIe Root Port Bridge
- Enables Root Complex on the HiFive Unleashed Board
- Stay tuned for FPGA developer versions
Microsemi Mi-V HiFive Unleashed Expansion Board
PolarFire Mi-V HiFive Unleashed Development Platform

- HDMI Type A
- USB Type A
- PCIe x1
- PCIe x16
- Power Supplies
- HDMI 1.4 PHY
- HDMI Type A
- USB 2.0 PHY
- DDR4 x16
- FlashPro 4
- LEDs
- Pushbutton
- OSC 50 MHz
- PCIe Root Complex
- Chip Link
- GMII
- SPI
- Power Tree
- Ethernet Switch
- MDI
- RJ45
- SiFive Motherboard
- JTAG
- SPI
- SPI Flash
- DDR4
- QSPI
- GbE PHY
- 64b+ECC
- SDCard
- SDCard
- PCIe Switch
- PCIe x4
- PCIe x1
- PCIe to SATA
- eMMC
- μSD
- μSD
- USB Type A
- CP2106
- CP2104
- USB PHY
- MAX3051
- QSPI
- DC Jack
- 120V~50 W
HiFive Unleashed + Unleashed Expansion Board
All the Peripherals You Need to Build a RISC-V PC
Tiny-YOLOv2

- Fully Convolutional Neural Network - 9 Convolutional Layers
  - convolution operation + batch normalisation + activation + pooling
- Trained end-to-end on Pascal VOC dataset
- Quantized and finetuned from provided base network by Joseph Redmon
  - Tiny YOLO @ https://pjreddie.com/darknet/yolo/

Core Deep Learning
an embedded FPGA solution
PolarFire Tiny Yolo Video
Core Deep Learning Block Diagram

Core Architecture

Core generator features

• Full pipeline from convolutional neural network description to FPGA implementation
• Network retraining for memory footprint minimisation
• Support for different network layers
  • Convolutional layer
  • Fully connected layer
  • Pooling layer
  • Activation layers
Mi-V RISC-V Soft CPU Summary

- A roadmap of soft CPUs for Microsemi FPGAs, royalty free
- Standardized ISA to protect your software investment
- Portable RTL for high-volume customers to migrate to an ASIC
- Security customers can inspect the RTL for trust
- Enables avionics and safety certification with viewable RTL
- Supported by industry-standard open-source tools

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Mi-V HiFive Unleashed Expansion Summary

- Accelerates the RISC-V Linux Ecosystem
- Enable the community to port tools, OS’s, middleware, packages to RISC-V
- Supporting the community supports our soft CPUs for our FPGAs
- Supporting the community supports the MI-V ecosystem and vice versa
- Deep Learning Core demo uses
  - Debian Linux, Xserver, OpenCV, V4L, PCIe and more were used
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