Introducing the Latest SiFive RISC-V Core IP Series

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SiFive RISC-V Core IP Product Offering

**SiFive RISC-V Core IP**

**E Cores**

- **E3/5Series**
  - High Performance Embedded
- **E2Series**
  - SiFive’s Most Efficient Series
  - Networking Industrial Modems
  - Microcontrollers IoT Wearables

**U Cores**

- **E51Standard Core**
- **E21Standard Core**
- **E20Standard Core**
- **E51Standard Core**

**Core Series** offer unique design points which can then be customized to meet application specific requirements

**Standard Cores** represent pre-configured implementations of a Core Series which are available for free RTL and FPGA evaluations
SiFive E3 and E5 Series RISC-V Core IP
June 2018 Update
SiFive E3 and E5 Series Overview

High Performance 32bit and 64bit RISC-V MCUs

• **New Pipelined Multiplication Unit**
  – Better performance: 3 Coremarks/MHz

• **Multicore Support**
  – Pre-integrated and verified by SiFive
  – Supports up to 8+ cores

• **Flexible Memory Architecture**
  – I-Cache can be reconfigured into I-Cache + ITIM
  – DTIM for fast on Core Complex Data Access (D-Cache option also available)
  – ECC/Parity Protection on all memories
  – Off Core Complex memory access through Memory, System and Peripheral Ports with configurable

• **Fast Interrupts**
  – Supports fast vectored local interrupts and shared global interrupts
  – E3/E5 with Interrupt Handlers in ITIM can enter a local interrupt ISR in as little as 10 cycles
  – Does not require separate integration with a separate interrupt controller

• **Memory Protection**
  – 8 region physical memory protection
  – Region locking

• **Evaluate Today**
  – E51 and E31 Standard Core RTL and FPGA evaluations are available now
Introducing SiFive E2 Series RISC-V Core IP
SiFive E2 Series RISC-V Core IP

• **SiFive’s Smallest, Lowest Power, Core Series**
  – Clean sheet design from the inventors of RISC-V
  – New interrupt controller enabling **fast** interrupt handling
  – Support for Heterogenous MP with other SiFive Cores

• **E2 Series Configurability**
  – **Core** – Tune the E2 for higher performance, or lower area
  – **Security** – Support for Memory Protection and RISC-V Machine and User Modes
  – **Memory Map** – Fully customizable memory map
  – **Ports** – Flexibility in the number and types of ports
  – And more – Interrupts, Debug and Trace, Memory Protection, Tightly Integrated Memory

• **E20 and E21 are Standard Cores within the E2 Series**
  – Standard Cores are benchmarked with published Power, Performance, and Area
  – RTL and FPGA evaluations are available

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**SiFive E2 Series RISC-V Core IP**

**E20 Core Complex**

**Industry leading 32-bit MCU efficiency:**
- Embedded Microcontroller
- IoT
- Analog Mixed Signal
- 8-bit replacement
- Programmable Finite State Machine

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**E21 Core Complex**

**Full featured 32-bit RISC-V MCU:**
- Sensor Fusion
- Wearables
- General Purpose Microcontroller
- Smart IoT
- Minion Core
- Smart Connected Toys
E2 Series Features

The Smallest, Most Efficient RISC-V MCU Family

- **E2 Series core architectural overview**
  - RV32IMACF capable core
  - 2-3 stage, optional, Harvard Pipeline

- **Configurable to meet application specific needs**
  - Ability to add multiple outbound Ports of different specifications
  - Optional Tightly Integrated Memory (TIM)
  - Flexible address map
  - Optional FPU, tunable Multiply performance, Memory Protection, and more...

- **First RISC-V core with support for the RISC-V Core Local Interrupt Controller (CLIC)**
  - Execute first instruction of a C handler in 6 cycles
  - Hardware interrupt prioritization and nesting

- **Drop In Cortex-M0+ and Cortex-M3/M4 replacement**
  - E21 has 12% more performance vs Cortex-M4
  - E20 has 28% more performance vs Cortex-M0+
Better than the Competition

- SiFive Standard Core outperform ARM equivalent cores
- E21 is 12% higher performance per MHz vs Cortex-M4 in CoreMark
  - When using equivalent GCC Compilers
- E20 is 28% higher performance per MHz vs Cortex-M0+ in CoreMark
  - When using equivalent GCC Compilers
- E2 Series Cores are also Area and Power Efficient
  - See details in the following slides
- E2 Series configurability allows for the core performance and area to be tuned to the exact application requirements
  - The E2 Series can be configured smaller than the E20 Standard Core
  - The E2 Series can be configured with more features than the E21 Standard Core
**E2 Series Memory Subsystem**

- **E2 Core can be configured with 1 or 2 bus interfaces**
  - 2 bus interfaces allows for simultaneous Instruction and Data accesses from the core giving higher performance

- **S-Bus is a highly optimized crossbar allowing for fast access the TIM banks and System Port**
  - Can have multiple parallel access: Fetching instructions from one TIM, while writing data to the other

- **Optional 2x TIM banks**
  - Guaranteed low latency access through the S-Bus
  - Supports parallel access to both TIM banks for E2 cores with 2 bus interface configurations

- **P-Bus supports On-Core Complex peripherals and the Peripheral Port**
  - Support for RISC-V Atomic instructions which can be used for single-cycle Read-Modify-Write operations

- **E2 Core Instruction and Data accesses can target any Port or TIM**
  - No pre-defined address map! Place instructions and data where it makes sense for your application

*Dotted lines represent optional interfaces/modules*
Core Local Interrupt Controller (CLIC)

- **Simplified interrupt scheme which allows for low latency interrupt servicing, hardware prioritization, and pre-emption**
  - Support for up to 1024 interrupts
  - Global programmable prioritization of all interrupts including software and timer
  - Works with E Cores and U Cores
  - Still supports PLIC for global interrupts shared with other cores in the SoC

- **Extreme low latency with support for Vectoring directly to ISR**
  - 6 cycles into first instruction of ISR, 18 cycles total to complete a simple ISR in an E2 Series Pipeline
  - Vector table contains function pointers (addresses) to ISR

- **Interrupt pre-emption capabilities**
  - Up to 16 levels of nesting, and programmable priority levels within each level

- **Easy to use programmers model**
  - GCC interrupt function attribute, no assembly necessary
  - Multiple SW interrupts with programmable priority levels
  - CLIC driver included in SiFive SDK for easy programmability
E21 Standard Core

- **Full Featured RISC-V MCU**
  - 0.037mm² in TSMC 28HPC for entire Core Complex without TIM RAMs
  - 1.38 DMIPS/MHz, 3.1 Coremarks/MHz

- **2 Core Interfaces**
  - Allows for simultaneous instruction and data access

- **Efficient memory system**
  - Banked TIM for fast local memory
  - Simultaneous Instruction and Data Accesses (Harvard Architecture)

- **User Mode and Physical Memory Protection (PMP)**
  - 4 Region PMP

- **4 Hardware breakpoint/watchpoints**

- **Extreme low latency interrupt handling**
  - Execute first instruction of C handler in 6 cycles
  - Execute entire ISR in 18 cycles

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**E21 (AHB-Lite) Post-Route Physical Design**

<table>
<thead>
<tr>
<th>Implementation Details</th>
<th>TSMC 28HPC</th>
<th>UMC 55LP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency @ worst setup corner</td>
<td>50MHz</td>
<td>585MHz</td>
</tr>
<tr>
<td>Worst Setup Corner</td>
<td>ssg_0p81v_m40c_cworst</td>
<td>ss_1p08v_125c_Cmax</td>
</tr>
<tr>
<td>Core Complex Area (mm²)*</td>
<td>0.037</td>
<td>0.077</td>
</tr>
<tr>
<td>Core Only Area (mm²)**</td>
<td>0.015</td>
<td>0.042</td>
</tr>
<tr>
<td>Core Complex Power – Dhrystones (mW) @ worst setup frequency</td>
<td>1.3</td>
<td>26</td>
</tr>
<tr>
<td>Power Characterization Corner</td>
<td>tt_0p9v_25c_typical</td>
<td>tt_1p2v_25c_Typ</td>
</tr>
</tbody>
</table>

Note: All area and power numbers do not include RAMs

*Core Complex includes the Core plus CLIC w/127 irq and 4 priority bits, Debug w/ 4 hw breakpoints, 4 Region PMP, TIM Logic, internal bus and ports
**Core only includes the core pipeline only
E20 Standard Core

- **SiFive’s Most Efficient Standard Core**
  - 0.023mm² in TSMC 28HPC for entire Core Complex including CLIC, Debug, and System Port
  - 1.1DMIPS/MHz, 2.4 Coremarks/MHz

- **E20 Standard Core is optimized for Area and Power**
  - Single Core Interface for all Instruction and Data accesses
  - 4 cycle hardware multiply
  - Single System Port Interface

- **4 Hardware breakpoint/watchpoints**

- **Extreme low latency interrupt handling**
  - Execute first instruction of C handler in 6 cycles
  - Execute entire ISR in 18 cycles
The E2 Series can be configured to meet your application requirements

<table>
<thead>
<tr>
<th>E2 Series Options</th>
<th>E20 Standard Core</th>
<th>E21 Standard Core</th>
<th>Cortex-M0+</th>
<th>Cortex-M3</th>
<th>Cortex-M4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dhrystone</td>
<td>Up to 1.38 DMIPS/MHz</td>
<td>1.1 DMIPS/MHz</td>
<td>1.38 DMIPS/MHz</td>
<td>0.95 DMIPS/MHz</td>
<td>1.25 DMIPS/MHz</td>
</tr>
<tr>
<td>CoreMark</td>
<td>Up to 3.1</td>
<td>2.4 CoreMarks/MHz</td>
<td>3.1 CoreMarks/MHz</td>
<td>1.8 CoreMarks/MHz</td>
<td>2.76 Coremarks/MHz</td>
</tr>
<tr>
<td>Integer Registers</td>
<td>31 Useable</td>
<td>31 Useable</td>
<td>31 Useable</td>
<td>13 Useable</td>
<td>13 Useable</td>
</tr>
<tr>
<td>FPU</td>
<td>Optional FPU</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Hardware Multiply and Divide</td>
<td>Yes, Optional</td>
<td>Yes</td>
<td>Yes</td>
<td>Hardware Multiply Only</td>
<td>Yes</td>
</tr>
<tr>
<td>Memory Map</td>
<td>Customizable</td>
<td>SiFive Freedom Platform</td>
<td>SiFive Freedom Platform</td>
<td>Fixed ARMv6-M</td>
<td>Fixed ARMv7-M</td>
</tr>
<tr>
<td>Atomics</td>
<td>Optional: RISC-V standard AMO support via Peripheral Port</td>
<td>No Peripheral Port</td>
<td>RISC-V AMO standard support via Peripheral Port</td>
<td>None</td>
<td>Bit-band and Load/Store Exclusive</td>
</tr>
<tr>
<td>Number of Interrupts</td>
<td>Up to 1024</td>
<td>32</td>
<td>127</td>
<td>32</td>
<td>240</td>
</tr>
<tr>
<td>Interrupt Latency into C Handler</td>
<td>6 Cycles – CLIC Vectored Mode</td>
<td>6 Cycles</td>
<td>6 Cycles</td>
<td>15 Cycles</td>
<td>12 Cycles</td>
</tr>
<tr>
<td>Memory Protection</td>
<td>Optional up to 8 Regions</td>
<td>N/A</td>
<td>4 Regions</td>
<td>Optional, ARMv6m</td>
<td>0 or 8 Region</td>
</tr>
<tr>
<td>Tightly Integrated Memory</td>
<td>Optional 2 Banks</td>
<td>None</td>
<td>2 Banks</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Bus Interfaces</td>
<td>Configurable: Up to 3 masters and 1 slave with support for TileLink, AXI, AHB-Lite, APB</td>
<td>1 Master</td>
<td>2 Master, 1 Slave</td>
<td>1 AHB-Lite</td>
<td>3 AHB-Lite</td>
</tr>
</tbody>
</table>

SiFive
End
E21 is 12% Higher Performance vs Cortex-M4

E21 outperforms the Cortex-M4 when using GCC

Compilers Versions
- SiFive – v201712
- ARM – gcc-arm-none-eabi-7-2017-q4-major

Dhrystone Compiler Flags
- SiFive
- ARM
  - cflags: -Wall -fmessage-length=0 -mno-sched-prolog -fno-builtin -ffunction-sections -fdata-sections -mfpu=fpv4-sp-d16 -mfloat-abi=softfp

Coremark Compiler Flags
- SiFive
- ARM

Cortex-M4 @19MHz w/FPU
E20 is 28% Higher Performance vs Cortex-M0+

E20 outperforms the Cortex-M4 when using GCC

Compilers Versions
- SiFive – v201712
- ARM – gcc-arm-none-eabi-7.2.1 (MCUExpresso default)

Dhrystone Compiler Flags
SiFive

ARM — https://developer.arm.com/products/processors/cortex-m/cortex-m0-plus

Coremark Compiler Flags
SiFive

ARM
cflags: -O2 -fno-common -g3 -Wall -c -fmessage-length=0 -fno-built-in -ffunction-sections -falign-functions=4 -falign-jumps=4 -falign-loops=4 -mno-sched-prolog -mcpu=cortex-m0plus -mthumb

Cortex-M0+ — NXP FRDM-KL25Z running at 48MHz