The Ultra-Low Power Open-source Core
to Accelerate the Spreading of RISC-V in China

bob_hu@nucleisys.com
June 2018
Agenda

- Personal Introduction
- The Status of RISC-V in China
- Our Passion of RISC-V in China
- Overview of Hummingbird E203 Core
- Details of Hummingbird E203 Core
- The Published 1st Chinese RISC-V Book
- The Board for Hummingbird E203
- The 2nd Coming Chinese RISC-V Book
- The Education Program for RISC-V
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Personal Introduction

Bob Hu  bob_hu@nucleisys.com

• Highlights
  • Over 10 years of ASIC design and verification experiences with 8 years of CPU industry experiences

• Education Background
  • Master of Microelectronics, Bachelor of EE, Shanghai Jiaotong University

• Work Experiences
  • 2018 ~ Now  Founder, Nuclei System Technology
  • 2017 ~ 2018  Processor Architect, Wuhan Silicon Integrated
  • 2016 ~ 2017  ASIC Director, Bitmain AI processor
  • 2012 ~ 2016  R&D Manager, Synopsys ARC processor IP
  • 2010 ~ 2012  Senior CPU Designer, Marvell
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The Status of RISC-V in China

Positive and Negative Status

• **Positive Status**
  • The ecosystem from industry and community growing very quickly in China Mainland
  • More and more people start to know RISC-V

• **Negative Status**
  • Very few people know RISC-V before year 2018
  • Very few people understand RISC-V
    • Many people even now treat RISC-V equal to another free and open-source Core
    • The most frequently asked question I heard is: *I heard there is a RISC-V, then where can I download that “free core”?* —— *Makes me dont know how to answer this question...*
    • Very few people can understand the profound effect of RISC-V to China semiconductor industry
  • Very few RISC-V cores developed by China player
  • Very few Chinese materials (include hardware and embedded software tools) for beginners
  • Very few Schools have already used RISC-V to educate in the classroom
  • Very few professional RISC-V processor IP company in China
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Our Passion of RISC-V in China

Our Passions and Contributions

- **Negative Situations**
  - Very few RISC-V cores developed by China player
  - Very few people know RISC-V before year 2018
  - Very few people understand RISC-V
  - Very few Chinese materials (include hardware and embedded software tools) for beginners
  - Very few Schools have already used RISC-V to educate (Starting Ongoing)
  - Very few professional RISC-V processor IP company in China

- **Our Works to Improve Them**
  - We developed and open-sourced Hummingbird E203 core
  - I Started a WeChat subscription number (微信公众号) to popularize RISC-V concepts
  - I published the 1st Chinese RISC-V book
  - I am ongoing to publish 2nd Chinese RISC-V book
  - We are promoting Hummingbird E203 into the education fields
  - We have established one start-up Company now!
Our Passion of RISC-V in China

The 1st open-source RISC-V Core from China Mainland

https://github.com/SI-RISCV/e200_opensource

Hummingbird E200 Opensource Processor Core

About

This repository hosts the project for open-source hummingbird E200 RISC processor Core.

The Hummingbird E200 core is a two-stage pipeline based ultra-low power/area implementation, which has both performance and area benchmarks better than ARM Cortex-M0+ core, making the Hummingbird E200 as a perfect replacement for legacy 8051 core or ARM Cortex-M cores in the IoT or other ultra-low power applications.

To boost the RISC-V popularity and to speed up the IoT development in China, we are very proud to make it open-source. It is the first open-source processor core from China mainland with industry level quality and state-of-art CPU design skills to support RISC-V instruction set.

Our ambition is to make “Hummingbird E200” become next 8051 in China, please go with us to make it happen.

Usages and Applications

The open-source Hummingbird E200 core can be a perfect candidate for the following fields:

- Replace legacy 8051 core for better performance.
- Replace Cortex-M core for lower cost.
- Also, the Hummingbird E200 core as a simple ultra-low power core and SoC, which is "袖手可及，五指俱全", with detailed Docs and Software/FPGA Demo, hence, it will be a perfect example for lab practice in university or entry-level studying.

Detailed Introduction

We have provided very detailed introduction and quick start-up documents to help you ramping it up.

The detailed introduction and the quick start documentation can be seen from e200_opensource/doc directory.

By following the guidelines from the doc, you can very easily start to use Hummingbird E200 processor core and demo SoC.
Our Passion of RISC-V in China

WeChat subscription number (微信公众号)
Our Passion of RISC-V in China

The 1st Chinese RISC-V Book in China

The book Introduced in: https://mp.weixin.qq.com/s/eECYepzO8c_FS_I9u2zIaA
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Overview of Hummingbird E203 Core

The 1st Open-Source RISC-V in China

- **Hummingbird Ultra-Low-Power Processor Core**
  - Ultra low-area 32bits RISC-V processor core
  - Two pipeline stages
  - Support RV32IMAC architecture
  - Area and Power in rival to Cortex M0/M0+/M3
  - Integrated ITCM (Instruction Tightly Coupled Memory) and DTCM (Data Tightly Coupled Memory)
  - Open-sourced in Github
    https://github.com/SI-RISCV/e200_opensource

- **Application Domains**
  - General or specified MCU core
  - Mix-signal Chip controller core
  - SoC controller core
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Details of Hummingbird E203 Core

**Pipeline Details**

- **Main Pipeline is two Stages**
  - Optimized for Area, timing and power

- ITCM and DTCM is integrated inside Core
Details of Hummingbird E203 Core

**Interfaces**

- **Master Interfaces**
  - Fast-IO Interface
  - System Bus Interface
  - Private Peripheral Interface
- **Slave Interface**
  - ITCM External Interface
  - DTCM External Interface
- **Interrupt Interface**
  - Interface with platform level interrupt controller
- **Debug Interface**
  - Interface with Debug-Module
# Details of Hummingbird E203 Core

## Comparison

- **Hummingbird E203 in Comparison with ARM Cortex M0/M0+**

<table>
<thead>
<tr>
<th></th>
<th>Cortex-M0</th>
<th>Cortex-M0+</th>
<th>Hummingbird E203</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dhrystone DMIPS/MHz</strong></td>
<td>0.84</td>
<td>0.93</td>
<td>1.23</td>
</tr>
<tr>
<td><strong>CoreMarks/MHz</strong></td>
<td>1.62</td>
<td>1.77</td>
<td>2.15</td>
</tr>
<tr>
<td><strong>Minimal Configuration (Gates)</strong></td>
<td>12K</td>
<td>12K</td>
<td>12K (Typical Config 18K)</td>
</tr>
<tr>
<td><strong>Pipeline Stages</strong></td>
<td>3 stages</td>
<td>2 stages</td>
<td>2 stages</td>
</tr>
<tr>
<td><strong>Hardware Multiplier</strong></td>
<td>Yes (Configurable for single-cycle or Multi-cycles implementations)</td>
<td>Yes (Multi-Cycles Implementation)</td>
<td></td>
</tr>
<tr>
<td><strong>Hardware Divider</strong></td>
<td>No</td>
<td></td>
<td>Yes (Multi-Cycles Implementation)</td>
</tr>
<tr>
<td><strong>ITCM and DTCM</strong></td>
<td>No embedded ITCM and DTCM, need customer to integrate by themselves</td>
<td>Provide embedded ITCM (64bits wide) and DTCM to easy customer</td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
- Besides open-sourced Hummingbird E203, there are commercial version (Nuclei N200 Series) which can contact Bob Hu by adding WeChat subscription number (微信公众号: 硅农亚历山大)
Details of Hummingbird E203 Core

**Features**

- **Instruction Set Architecture Features:**
  - Supporting architecture RV32IMAC
  - Supporting Machine Mode Only
  - Supporting Interrupts, PLIC, Timer

- **Highlighted Open-source Features**
  - Basic JTAG interactive debug support
  - Together with typical fully SoC open-sourced
  - FPGA demo supported with detailed doc
  - Embedded software SDK and demo provided

**Note:**
- Will be introduced later with more details
Details of Hummingbird E203 Core

*Interfaces Protocol*

- The open-source version use **Self-defined ICB interface**
  - Very simple, combined the merits of AHB and AXI, very easy to be converted to AHB/AXI/APB

- **NOTE:**
  - The commercial version provide AHB/AXI/APB interfaces configurable
The EAI (Extended Accelerator Interface)

- Four Channels protocol defined
- Extended Instruction accelerator just need to follow the protocol
- The extended Instructions can just use the reserved “custom” instructions inline into the C/C++ program, no need to change the compiler toolchain

Note:
- The EAI Interface is not yet open-sourced (the intern student is wanted)
- The commercial version provide EAI
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### Contents of Book

- All Other Detailed Information can be seen from the book

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<thead>
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<th>CPU 与 RISC-V 综述</th>
</tr>
</thead>
<tbody>
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<td>一文读懂 CPU 之三生三世——2</td>
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The Board for Hummingbird E203

**FPGA-based MCU Board**

- Xilinx FPGA based MCU Board (<399~1299RMB)
The Board for Hummingbird E203

**FPGA-based MCU Board**

- **Anlogic (上海安路)** FPGA based MCU Board (<100RMB)
- **PANGO (紫光同创)** FPGA based MCU Board (<100RMB)

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**Lichee Tang**

- **FPC 40P座** (可接RGB LCD, VGA转换板，高速DAC模快)
- **用户自选 flash** (支持Nor/ Nand)
- **自弹式TF卡座**
- **双排插针间距900mil** (兼容普通板开发)
- **整板引出130+ IO** (半孔引出额外IO)
- **相邻插针LVDS等长引出**
- **引出8路GCLK**
- **全引出8路ADC**

**IC接口**

- **电阻触摸屏接口** (配合RGB LCD使用)

**安路FPGA**

- (20K LE, 约130KB SRAM, 丰富的Jds引脚, 内置ADC)

**FPC24P座** (接DVP摄像头，高速ADC模快)

**3路DCDC电源芯片**

(稳定高效的电源供应，bank0 IO电平独立可调)

**板载FPGA JTAG下载调试器**

(左：状态指示灯，右：电源指示灯)

**插脚型 micro-usb 接口**

(左：复位按键，右：用户按键)

**RGB LED**

**52Pin mini-PCI 金手指接口**

(不挑PCB层时使用)
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The next coming 2\textsuperscript{nd} Chinese RISC-V Book

Contents of Book

- The 1\textsuperscript{st} book is to spread RISC-V by detailed introduction of E203 Core
  - Targeting for hardware Chip designer

- The 2\textsuperscript{nd} book is to introduce how to use RISC-V for embedded software development
  - Targeting the embedded software programmer
  - This is even more important because most of the people are the user, who are not interested into designing CPU but just using CPU
  - Will be firstly opened in the WeChat subscription number (微信公众号：硅农亚历山大)
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The Education Program for RISC-V

*Education Program*

- Provide the trainings for beginners
  - .......

- Promote the open-source Hummingbird E203 into the Classroom of Chinese University
  - With books
  - With boards
  - With the pre-designed class contents
  - Conduct the contests and club
  - ...
  - ...
  - Thinking very hard.... 😞 😒 Need help.....
  - ....
Q & A

Thanks
Nuclei N200 Series
RISC-V Core IP Introduction

Bob Hu
June 2018
Company Introduction

● Our Missions
  • To be a RISC-V processor core vendor based on China Mainland
  • Enable Chinese semiconductor industry with RISC-V Core with China Mainland Domestic Autonomy (国产自主可控) and better local service

● Business Scope
  • RISC-V processor core IP licensing
  • RISC-V processor core and subsystem customization

● Highlights
  • Hummingbird E203 processor core with ultra low-area/power features, launched at 2017 (1st RISC-V from China Mainland) targeting to Deeply-embedded and IoT domains
  • Nuclei N200 series included the N203, N205, N207
  • The measured data from real silicon chip proved the better power consumptions over rival Cortex-M core
  • Perfect replacements to ARM Cortex-M processor cores with lower royalties
# Nuclei N200 Overall Introduction

## N200 Processor Core Series

### Nuclei N200 Series Features and Comparison

<table>
<thead>
<tr>
<th></th>
<th>N203</th>
<th>N205</th>
<th>N205f</th>
<th>N205fd</th>
<th>N207</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RISC-V Arch</strong></td>
<td>RV32IMAC</td>
<td>RV32IMAC</td>
<td>RV32IMAFC</td>
<td>RV32IMAFDC</td>
<td>RV32IMAC</td>
</tr>
<tr>
<td><strong>Hardware</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Configurable</td>
</tr>
<tr>
<td><strong>Multiplier/Divider</strong></td>
<td>17 cycle Multiplier</td>
<td>1 cycle Multiplier</td>
<td>33 cycles divider</td>
<td>33 cycles divider</td>
<td></td>
</tr>
<tr>
<td><strong>Single-precision FPU</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Configurable</td>
</tr>
<tr>
<td><strong>Double-precision FPU</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Configurable</td>
</tr>
<tr>
<td><strong>ICache</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

- **Low-power core with ICache to easy SIP with Nor Flash**
- **Replace ARM Cortex-M4F/M7 for double-precision floating-point**

---

**Replace ARM Cortex M0/M0+/M3**

**Replace ARM Cortex-M4F for single-precision floating-point**
## The Merits of Commercial Version

<table>
<thead>
<tr>
<th>Feature</th>
<th>E203 Open Source Version</th>
<th>N200 Commercial Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Full features of JTAG debugging</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>• Quality and Service Warrant</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>• Optimization of Area and performance</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>• Hierarchical Structure for Easier Integration</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>• Standard AMBA Bus Interface</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>• Extending Interface for Co-Processors</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>• Dual Lines Debugging Interfaces</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>• Fast Vector Nested Interrupt Controller</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>• Multiple-Privilege Levels and MPU</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>• Unaligned Load/Store handled by Hardware</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
## Nuclei N200 Overall Introduction

### N200 Processor Core Series over ARM

- **Nuclei N200 Series in Comparison with ARM Cortex-M Series**

<table>
<thead>
<tr>
<th></th>
<th>Cortex-M0</th>
<th>Cortex-M0+</th>
<th>Cortex-M3</th>
<th>Cortex-M4F</th>
<th>N203</th>
<th>N205</th>
<th>N205f</th>
<th>N205fd</th>
<th>N207</th>
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<td>2.15</td>
<td>3.36</td>
<td>3.40</td>
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<td>3.36~3.40</td>
</tr>
<tr>
<td><strong>Minimal Config (Gates)</strong></td>
<td>12K</td>
<td>12K</td>
<td>36K</td>
<td>90K</td>
<td>12K</td>
<td>20K</td>
<td>60K</td>
<td>90K</td>
<td>Configurable</td>
</tr>
<tr>
<td><strong>Pipeline Stages</strong></td>
<td>3 stages</td>
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<td>3 stages</td>
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<td>2 stages</td>
<td>2 stages</td>
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<td>2 stages</td>
</tr>
<tr>
<td><strong>Hardware Multiplier</strong></td>
<td>Yes (1-cycle or Multi-cycles)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes (Multi-cycles)</td>
<td>Yes (1-cycle)</td>
<td>Yes (1-cycle)</td>
<td>Yes (1-cycle)</td>
<td>Yes (1-cycle)</td>
<td>Yes (1-cycle)</td>
</tr>
<tr>
<td><strong>Hardware Divider</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Single-precision FPU</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Configurable</td>
</tr>
<tr>
<td><strong>Double-precision FPU</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Configurable</td>
</tr>
<tr>
<td><strong>DSP Extension</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Support user define and extendable</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Instruction Cache</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>ITCM and DTCM</strong></td>
<td>No embedded ITCM and DTCM, need customer to integrate by themselves</td>
<td>Provide embedded ITCM (64bits wide) and DTCM to easy customer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ECC protection to ITCM/DTCM</strong></td>
<td>Need customer to implement by themselves</td>
<td>Provide ECC protection to ITCM and DTCM</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Extendibility</strong></td>
<td>No</td>
<td>Support user to extend instructions</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>
Nuclei N205 Core Introduction

• **Features**
  - Based on 2 stage pipeline implementations
  - Area in rival to Cortex-M0+, performance in rival to Cortex-M3
  - Provided embedded Tightly Couple Memories ITCM and DTCM with ECC protection supported
  - Provide dedicated instruction interface to support eFlash or another ITCM2

• **Strengths**
  - **Support User-Expendability** (e.g., user defined DSP operation)
  - Perfect Replacement to ARM Cortex-M3
    - Better Performance
    - Smaller Areas
    - Lower Royalty Fees
**Nuclei N207 Core Introduction**

### Features

In addition to N205 features:
- Added ICache (2-Way, 32Bytes Cache Line Size, Cache-Size configurable)
- Added Configurable DCache (2-Way, 32Bytes Cache Line Size, Cache-Size configurable)

### Strengths

In addition to N205 features:
- Utilize the ICache, use SIP package external Nor-flash, to reach better flexibility and cost
- The ITCM size can be reduced, the eFlash can be eliminated to reduce die cost
- Note: The critical instruction can still be put in on-chip ITCM (but with smaller size)
Tool-chain and Software Development Environment

- **C/C++ Compiler**
  - Standard GNU GCC Toolchain (with both Linux and Windows version)

- **Software Development Kit**
  - Hbird-E-SDK: based on GCC Toolchain

- **Windows and Linux IDE**
  - Eclipse C/C++ Development IDE
  - Note: utilize the whole RISC-V ecosystem, any IDE supporting RISC-V will support Hummingbird E200 (because of standard ISA)

- **Software Simulation**
  - Based on QEMU

- **JTAG Debugger**
  - JTAG Debugger (USB-Disk size, Cost around 30 RMB)

- **RTOS Support**
  - FreeRTOS
  - RT-Thread
  - Note: utilize the whole RISC-V ecosystem, any RTOS supporting RISC-V will support Hummingbird E200 (because of standard ISA)
Q & A

Thanks

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