Core Deep Learning with HiFive Unleashed Expansion Kit

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Agenda

- Introduction to Mi-V Ecosystem

- Mi-V HiFive Unleashed Expansion Board
  - Hardware
  - Tools

- Deep Learning with Microsemi FPGA and RISC-V
  - Setup
  - Convolutional Neural Network Overview
  - Microsemi FPGA Advantage
  - Deep Learning Demo
Microsemi Invests In The RISC-V Ecosystem

- The Mi-V™ RISC-V ecosystem is a continually expanding comprehensive suite of tools and design resources to fully support RISC-V designs.

- Mi-V™ ecosystem aims to increase adoption of RISC-V ISA and Microsemi's soft CPU product family.

- Introduced the first soft CPUs for FPGAs

- Mi-V ecosystem enabled numerous RTOS
## CPUs: Mi-V Soft CPU Roadmap

<table>
<thead>
<tr>
<th>Core</th>
<th>LE's</th>
<th>CoreMark</th>
<th>Cache</th>
<th>Mul/Div</th>
<th>Floating Point</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>CORE_RISCV_AXI4</td>
<td>10K</td>
<td>2.01</td>
<td>8K I and D</td>
<td>Yes</td>
<td>N/A</td>
<td>Now</td>
</tr>
<tr>
<td>Mi_V_RV32IMA_L1_AHB</td>
<td>10K</td>
<td>2.01</td>
<td>8K I and D</td>
<td>Yes</td>
<td>N/A</td>
<td>Now</td>
</tr>
<tr>
<td>Mi_V_RV32IMAF_L1_AHB</td>
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<td>2.01</td>
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<tr>
<td>Mi_V_RV32I_AHB</td>
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<td>-</td>
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<td>N/A</td>
<td>N/A</td>
<td>Q2’18</td>
</tr>
<tr>
<td>Mi_V_RV32IMA_L1_AXI</td>
<td>10K</td>
<td>2.01</td>
<td>8K I and D</td>
<td>Yes</td>
<td>N/A</td>
<td>Q2’18</td>
</tr>
</tbody>
</table>

- **Mi_V_RV32I_AHB**
  - Small core, with debug, 4K LE’s

- Additional cores can be added based on customer demand
Mi-V Eclipse Based IDE

- A single tool chain for RISC-V and ARM MCUs
  - Easy migration from ARM to RISC-V
- Running on Linux or Windows Hosts
- Bundled with example projects and RTOSs
- https://github.com/RISCV-on-Microsemi-FPGA
Firmware Catalog

- Drivers for Microsemi RISC-V Soft CPUs
  - Updates pushed to your desktop
  - Release notes
  - User guides

- Version Controlled

- MISRA/Netrino compliant
Mi-V RISC-V Soft CPU RTOS Support Available Today

- **Open Source**
  - FreeRTOS
  - Huawei LiteOS
  - MyNewt
  - Zephyr

- **Commercial**
  - Express Logic - ThreadX
  - SiLabs - Micrium µC/OS III
  - Segger - embOS

*These RTOS already run on the Mi-V soft RISC-V CPUs*
Solutions: Example Designs on Github

- Design examples targeted to various boards
  - Hello world printf via UART
  - Interrupt blinky
  - Touch screen Tic-tac-toe
  - Crypto processor with RISC-V

- Getting started building a RISC-V tutorial

Repository: Microsemi
http://www.microsemi.com

- MPF300T-PolarFire-Eval-Kit
  PolarFire FPGA sample RISC-V designs
  - Verilog
  - 1 star
  - 3 forks
  - Updated on Jul 13

SoftConsole
Eclipse based IDE for RISC-V bare metal software development.
Mi-V Development and Evaluation Boards

Microsemi PolarFire Eval Kit (Price $1495) MPF300-EVAL-KIT_ES

Microsemi PolarFire Splash Kit (Price $699) MPF300-SPLASH-KIT-ES

Microsemi RTG4 Development Kit

Future Avalanche Board (Price $179) AVMPF300TS-01

Future RISCV Board (Price $99) FUTUREM2GL-EVB

Arrow Everest Board (Price $499) EVEREST-DEV-BOARD
Mi-V HiFive Unleashed Expansion: Advancing the Ecosystem

- Enables the community to port tools, OS’s, middleware, packages to RISC-V
- Makes software development easier
- Enables standard and custom peripherals

• Supporting the community supports our soft CPUs for our FPGAs
• Supporting the community supports the Mi-V ecosystem and vice versa
PolarFire HiFive Unleashed Development Platform

- Designed for Expandability
- Pre-programmed with a ChipLink to PCIe Root Port Bridge
- Enables Root Complex on the HiFive Unleashed Board
- Stay tuned for FPGA developer versions
PolarFire Mi-V HiFive Unleashed Development Platform
HiFive Unleashed + Unleashed Expansion Board
Resources

- **Microsemi docs**
  - https://www.microsemi.com/hifive-unleashed-expansion-board

- **Sifive Docs**

- **SiFive Forum**
  - https://forums.sifive.com/c/hifive-unleashed

- **SiFive Freedom Unleashed SDK**
  - https://github.com/sifive/freedom-u-sdk
Where to Buy?

- CrowdSupply – **Sold-out**
  - [https://www.crowdsupply.com/microsemi/hifive-unleashed-expansion-board](https://www.crowdsupply.com/microsemi/hifive-unleashed-expansion-board)

- New campaign under plan

- For immediate needs, please contact me
  - krishnakumar.r@microsemi.com
Deep Learning using Microsemi FPGA and RISC-V
Inference Setup

Input data → Trained Model → Prediction
Deep Learning Setup

- **Training data**
  - Database

- **Training algorithm**
  - Computer

- **Model**
  - Human head

- **Network training**
- **Evaluate**
- **Prediction**
- **Inference**
Convolutional Neural Networks (CNNs)

Traditional Image Processing Pipeline

Input

1. Hand-Crafted
   SIFT, HOG, Gabor Filters etc.
   Feature Extractor

2. Trainable
   Classfier

Output

- Pedestrian
- Car
- Animal
- Road

- Traditionally hand-crafted features
- Time consuming design
- Application Specific

Deep Learning

Input

1. Trainable
   Convolutional
   Layers with optional pooling and activation functions
   Feature Extractor

2. Trainable
   Classfier

Output

- Pedestrian
- Car
- Animal
- Road

- Deep Learning
  - Feature Learning
  - Trainable Feature Extractor
  - Requires lots of training data

- Became viable with improvements in
  - Training Techniques
  - Availability of Training Data
  - Processing power
Deep Learning Model
The Microsemi FPGAs Advantage
CNN Complexity

You Only Look Once: Redmon et al, 2016
CNN Complexity Overview

**Computation complexity**

<table>
<thead>
<tr>
<th>Layer operations (GOP)</th>
<th>Convolution layers</th>
<th>Fully connected layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.040</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>5.549</td>
<td>7</td>
</tr>
<tr>
<td>3</td>
<td>3.699</td>
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</tr>
<tr>
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<td>7</td>
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<tr>
<td>7</td>
<td>0.006</td>
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</tbody>
</table>

**External memory access**

<table>
<thead>
<tr>
<th>Weights required (Million)</th>
<th>Convolution layers</th>
<th>Fully connected layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.005</td>
<td>6</td>
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<tr>
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<td>0.442</td>
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<td>3</td>
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<td>5</td>
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</tr>
<tr>
<td>7</td>
<td>6.021</td>
<td></td>
</tr>
</tbody>
</table>
Dot Product Matrix Computation

\[ o_j = a_1 * w_{11} + a_1 * w_{12} + a_1 * w_{13} + \ldots + a_2 * w_{21} + a_2 * w_{22} + a_2 * w_{23} + \ldots \]

Figure: Math Block in PolarFire
CDL Design Space Exploration

- Implementation can either be computation-bounded or memory-bounded
- Model performance to off-chip memory traffic

\[ \text{Att Perf} = \min \left\{ \frac{\text{Computational roof}}{\text{CTC ration} \times \text{BW}} \right\} \]
A Scalable Solution

Watt  FPS  LEs
## Tiny YOLO v2.0 – PolarFire vs Zynq US+

<table>
<thead>
<tr>
<th>Parameters</th>
<th>PolarFire</th>
<th>Zynq UltraScale+</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame Rate</td>
<td>30fps</td>
<td>16fps</td>
</tr>
<tr>
<td>Device Power</td>
<td>3.5W</td>
<td>6W</td>
</tr>
<tr>
<td>mAP (mean average precision score)</td>
<td>45.1</td>
<td>48.5</td>
</tr>
<tr>
<td>Operating Frequency</td>
<td>200MHz</td>
<td>n/a</td>
</tr>
</tbody>
</table>
Microsemi’s Advantage in Deep Learning Summary

- Higher processing power due to efficient math block
- Low power consumption
- Scalable Deep Learning design provides optimum performance for available resources
PolarFire Tiny Yolo Video
Thank You

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