CPU Project in Western Digital: From Embedded Cores for Flash Controllers to Vision of Datacenter Processors with Open Interfaces

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December 4th, 2018
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Agenda

• Enterprise datacenter RISC-V CPU vision – all about open interfaces:
  – RISC-V multi-core
  – NVDIMM-P memory interfaces
  – Accelerator interfaces (PCIe, OpenCAPI)
  – OmniXtend™ – memory protocol interface enabling memory centric architectures

• Planned open source contributions

• Western Digital first core SweRV™:
  – Microarchitecture introduction
  – Performance benchmarks

• OmniXtend™ protocol:
Vision of RISC-V open architecture datacenter CPU

It is all about open interfaces
Vision for future datacenter CPU architecture

- Multi-threaded, multi-core CPU:
  - 1) Medium performance, OOO RISC-V Core for general purpose OS and software applications
  - 2) Standardized and open JEDEC interface architecture (NVDIMM-P) for high density emerging non-volatile memories
  - 3) Support for high bandwidth and low latency accelerator interfaces:
    - Supporting machine learning and inference engine accelerators
  - 4) Support for standardized memory protocol fabric – e.g. OmniXtend - Tilelink over 802.3:
    - Allowing coherent scale-out for memory-centric architectures
Memory-centric architecture with OmniXtend

- Allows large numbers of RISC-V compute nodes to connect to universally shared memory (NUMA) – standardized and open coherence protocols
- Enables memory appliance, aggregation/disaggregation
Memory-centric architecture with OmniXtend

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#LetDataThrive
Planned open source contributions

Subject to internal approvals

- Production grade instruction set simulator SweRV ISS™ (December 4th 2018):
  - https://github.com/westerndigitalcorporation/swerv-ISS
- RTL of the 2-way superscalar Western Digital SweRV Core™ (January 24th 2019):
  - https://github.com/westerndigitalcorporation/swerv
- OmniXtend reference implementations:
  - https://github.com/westerndigitalcorporation/omnixtend
  - Specification (December 4th 2018)
  - Switch P4 implementation (t.b.d)
  - Board designs (t.b.d)
- RISC-V Firmware development toolchain
SweRV Core™: Western Digital’s First RISC-V Core

Robert Golla
SweRV Core™ Complex

- **RISCV 32IMC Core**
  - First internally developed RISCV core

- **RISCV debug support**

- **Programmable Interrupt Controller**
  - Support for up to 255 external interrupts

- **AHB-lite, AXI bus support**

- **Frequency target**
  - 1 GHz at SSG process corner

- **Technology**
  - TSMC 28 nm
SweRV Core Microarchitecture

- 9 stage pipeline
- 4 stall points
  - Fetch1
    - Cache misses, line fills
  - Align
    - Form instructions from 3 fetch buffers
  - Decode
    - Decode up to 2 instructions from 4 instruction buffers
  - Commit
    - Commit up to 2 instructions / cycle
- EX pipes
  - ALU ops statically assigned to I0, I1 pipes
  - ALU's are symmetric
- Load/store pipe
  - Load-to-use of 2
- Multiply pipe
  - 3 cycle latency
- Divide pipe
  - 34 cycles, out-of-pipe
SweRV Core Branch Prediction / Branch Handling

- Branch direction is predicted using GSHARE algorithm
  - XOR of global branch history and PC
    - Used to lookup branch direction in branch history table (BHT)
  - PC hash
    - Used to lookup branch target in branch target table (BTB)
- Branches that hit in the BTB result in 1 cycle branch penalty
- Branches that mispredict in primary alu’s result in 4 cycle branch penalty
- Branches that mispredict in secondary alu’s result in 7 cycle branch penalty
SweRV Core Physical Design

• TSMC 28 nm
  – 125 C, SVT, 150 ps clock skew

• SSG corner w/out memories
  – 1 GHZ
    • .132 mm²
  – 800 MHZ
    • .100 mm²
  – 500 MHZ
    • .093 mm²

• TT corner w/out memories
  – 1 GHZ
    • .092 mm²
  – 800 MHZ
    • .091 mm²
  – 500 MHZ
    • .088 mm²
• 4.9 CoreMark/MHz
  – Additional performance gains are possible with compiler optimizations
  – Multi-threaded/multi-core results are always renormalized to a single execution context

• 2.9 Dhrystone MIPs/MHz
  – Using optimized strcpy function

CoreMark data from C.Celio, D.Patterson, K.Asanovic,https://www2.eecs.berkeley.edu/Pubs/TechRpts/2015/EECS-2015-167.pdf
Driving Momentum

Western Digital ships in excess of 1 Billion cores per year ...and we expect to double that.
OmniXtend™: direct to caches over commodity fabric

Dejan Vucinic

Western Digital
Emergence of memory fabric

Memory fabric may mean different things to different people:

- Page fault trap leading to RDMA request (incurs context switch and SW overhead)
- Global address translation management in SW, leading to LD/ST across global memory fabric
- Coherence protocol scaled out, global page management and no context switching
Memory-centric architecture with OmniXtend

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OmniXtend memory-centric fabric architecture

- Replaces Ethernet L2 with serialized TileLink messages
  - Keeps standard 802.3 L1 frame, interoperates with Barefoot Tofino and future OTS Ethernet switches
  - Custom frames are parsed and processed in P4 language
  - Enables stateful message processing inside the switching fabric
  - Supports innovation required for RAS
  - FPGA or ASIC switch; not limited to 802.3

- Protocol translation and modification inside fabric:
  - Requires no new silicon

- 100 Gb/s is available today
  - Clear roadmap to 200 and 400 with 56Gb PAM4 and x8
P4 example: OmniXtend programmable switch

• Barefoot Tofino ASIC (or FPGA with e.g. Xilinx SDNet):
  – 64-port 100 GigE switch, 6.4 Tbit/s aggregate throughput, < 400 ns latency
  – Supports P4 HDL, successor to OpenFlow enabling protocol innovation
  – Describe TileLink message format in P4
  – Match-Action Pipeline (a.k.a. “flow tables”) enables line-rate performance
  – Modifications to coherence domains, protocols require no new silicon
Memory fabric protocol OmniXtend innovation platform
NAND Controller SoC applications

- Multi-purpose SoC for consumer SSD applications
- First RISC-V based SoC for NAND controller applications
- Advantages:
  - Full advantage of open source software ecosystem for RISC-V
  - Instruction optimization for NAND media handling
  - Freedom of power and performance optimization for end application