SiFive Freedom Revolution

Krste Asanovic, Co-Founder and Chief Architect
SiFive Freedom Chip Platforms

• Customer designs custom SoC by combining:
  – Pre-integrated configurable base SoC architecture
    • Processors, interconnect, on-chip IP, off-chip interfaces
  – Catalog of SiFive + DesignShare partner IP
  – Customer IP

• Each platform built for specific technology

• Two SiFive chip platforms previously announced:
  – Freedom Everywhere, TSMC 180nm
  – Freedom Unleashed, TSMC 28nm
Freedom Everywhere 32-bit Low-power microcontroller platform

- **320+ MHz SiFive E31 CPU**
  - 16KB L1$, 16KB Data Scratchpad
  - Hardware Multiply/Divide, Debug Module
- **Multiple Power Domains**
- **Low-Power Standby**
- **Wide Range of Clock Inputs**

**SiFive**

Freedom E310, QFN48, manufactured in TSMC 180nm
HiFive1: Arduino-Compatible RISC-V Dev Board

- SiFive FE310-G000 (built in 180nm)
- Operating Voltage: 3.3 V and 1.8 V
- Input Voltage: 5 V USB or 7-12 VDC Jack
- IO Voltages: Both 3.3 V or 5 V supported
- Digital I/O Pins: 19
- PWM Pins: 9
- SPI Controllers/HW CS Pins: 1/3
- External Interrupt Pins: 19
- External Wakeup Pins: 1
- Flash Memory: 16 MB Quad SPI
- Host Interface (microUSB): Program, Debug, and Serial Communication

Sold out, refresh coming soon!
Freedom Everywhere Example Tapeouts

- TSMC 180nm
- E2 series and E3 series cores
- AlwaysOn, PMU
- Scratchpad and/or caches
- Analog and digital I/O
- Alternate power supplies
Freedom Unleashed 64-bit Multi-Core RISC-V Linux Platform

- 1.5+ GHz U54-MC SiFive CPU
  - 1x E51: 16KB L1I$, 8KB DTIM with ECC support
  - 4x U54: 32KB L1I$, 32KB L1D$ with ECC support
  - Single- and Double-precision floating-point support
  - 2MB Banked L2$ with directory-based cache-coherence & ECC support
- ChipLink
  - Serialized Chip-to-Chip Coherent TileLink Interconnect
- DDR3/4, GbE, Peripherals

Freedom U540, FCBGA, manufactured in TSMC 28nm
HiFive Unleashed: World’s First Multi-Core RISC-V Linux Dev Board

- SiFive FU540-C000 (built in 28nm)
- 8 GB 64-bit DDR4 with ECC
- Gigabit Ethernet Port
- 32 MB Quad SPI Flash
- MicroSD card for removable storage
- MicroUSB for debug and serial communication
- Digital GPIO pins
- FMC connector for future expansion with add-in cards

Order for December delivery at crowdsupply.com for $999
Chip Templates: Pre-configured SoC starting points

FE  Freedom Everywhere
Designed for embedded microcontrollers, IoT, wearables, and more.

- TSMC 180nm process

Low Power MCU
General-purpose embedded MCU

Intelligent Sensor
Hub for analog & digital sensors

U2F Security Key
Key for 2-factor authentication

FU  Freedom Unleashed
Unix-capable SoCs suitable for machine learning, storage, networking, and more.

- TSMC 28nm process

Application Processor
Linux-ready with DDR3/DDR4 controller

SSD Controller
High performance NVMe FLASH controller

AI Camera SoC
Intelligent deep neural network camera processor

Chip Designer Preview at sifive.com
SiFive Freedom Revolution

- High-bandwidth AI and networking applications in TSMC 16nm
- SiFive 7-series RISC-V processors with vector units
- Cache-coherent TileLink interconnect
- 2.4 Gb/s HBM2 memory interface
- 28-56-112 Gb/s SerDes links (from partner Credo)
- Interlaken chip-chip protocol
- High-speed 40+Gb/s Ethernet
Freedom Revolution Platform Template

PCIe Gen3/4
SerDes
SPI, UART, GPIO
SerDes
Ethernet

Digital I/O
Network I/O
Debug/Trace

Host Interface

Executive Tile

L1-I$
U7 Core
L1-D$

L2-U$

Compute Tile

S7 Core(s)
DMA
Custom Accelerator

TileLink
SRAM

Custom Compute Array

Compute Tile

InterLaken Chip-Chip
TileLink Serializer

TileLink Coherent Cross-Chip Fabric

HBM Channel Controller

HBM Channel Controller

HBM Channel Controller

TileLink cache coherent chip-chip interconnect
HBM2 Phy + Controller

- Silicon-Proven in TSMC 16nm
- TSMC’s OIP Ecosystem Forum 2017 Customers’ Choice Award for best paper “HBM2”

- Total bandwidth: >300GB/s
- Data transfer: 1.6-2.4 Gb/s
- SiP TSMC CoWoS (2.5D)
- Interposer TSMC 65nm
- Interposer trace length < 5mm
- Supports all HBM stack vendors

- IP available now
- Several licensees to date
Next-Generation HBM2 IP Subsystem

AXI-based or TileLink-based HBM2 IP subsystem development

Targeting 3.2 Gbps per-pin data rates, and beyond, in TSMC’s latest 7nm FinFET technologies

- Supports up to 3.2 Gbps/pin data rates and beyond
- Supports up to 8 channels (16 pseudo channels)
- Supports up to >400GBytes of total bandwidth
- Supports full DFI4.0 compliant controller and PHY interface
- Supports multi-port AXI interface or TileLink
- Supports different schemes of arbitration and scheduling (QoS)
- Supports different address mapping modes
Interlaken IP Subsystem

- **High Speed**
- **Channelized Packet Interface**
- **Highly Scalable**
- **Low Latency**

Works with up to 48 parallel physical SerDes lanes 3.125 Gbps to 56 Gbps speeds

Supports bandwidth of up to 1.2 Tbps

Configurable user interface of 128/256 bit width

Interlaken IP 75+ licensees to date, over 10+ years

ASIC/FPGA

Interlaken IP placement in the chip

ASCI/FPGA
Channelized MAC IP supports 400/200/100/50/25/10GE client port

FlexE IP is fully compliant to OIF Flex Ethernet Standard v1.1

PCS IP supports IEEE standard 802.3 for 10G/25G/40G/50G/100G/200G/400G data rates

MCMR FEC (Forward Error Correction) IP supports Ethernet standard with up to 400G data rates

Flow-Based Client Interface

- Flow-Based Client Interface
- ODU Interface
- MCMR FEC & PMA
- PHY

Ethernet IP Subsystem
MAC IP + PCS IP + MCMR FEC IP
SiFive for IP components, or entire custom SoC

Available:

- RISC-V U7 and S7 series Core IP
- TileLink on-chip coherent fabric
- TileLink chip-chip coherent serialization (see demo with WDC)
- 2.4 Gb/s HBM2 phy and controller in TSMC 16nm FFC
- 56-112Gb/s SerDes in TSMC 16nm and 7nm (from partner Credo)
- Interlaken IP
- Ethernet IP

In development:

- E7/U7 vector and custom extensions
- 3.2 Gb/s HBM2 in 7nm
- Higher-performance RISC-V processors

Please come talk to us for your RISC-V AI chip needs!