Deepening the RISC-V Ecosystem to Drive Industry-wide Adoption

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NXP - Why are we a Platinum Member

Encourage University & Corporate Research

Influence Roadmap for the benefit all

We want to be with you at the forefront of this revolutionary technology!
Facilitate a Deep Ecosystem
Drive New Architectural & Software Innovations
A Deep Ecosystem is NOT …
Announcements with unrealizable promises
where financial gain is the primary motivation
A Deep Ecosystem is ...
(from a semiconductor vendor POV)
Fragmentation leads to stagnation

Let's facilitate growth with ‘un-fragmentation’ working group
Enable Sustainable Growth Environment

• Demand quality tool offerings to ensure reliable product development

• Consolidate ISA Extensions important to get strong ecosystem partners
Join the Open-ISA Community

• One site for all Open-source ISA enthusiasts
• Open-ISA’s Role → Expand RISC-V Ecosystem
• Developers sharing ideas & experiences …
• Discussion board …
• Open to any and all relevant ecosystem partners
• Order VEGAboard & download documentation …
VEGAbroid - Full-Featured RISC-V Secure Connected Platform

- Built by open-source enthusiasts in Software R&D and Systems / Applications Engineers
- Intended only as silicon evaluation vehicle
- SoC – NOT FOR SALE!
Meet the VEGAboard: a hardware platform with two RISC-V cores and everything you need to <create> the next big thing.
VEGAbboard Supports

• Full suite of middleware and communication stacks (e.g. BLE)
• Arduino connector to access 1000s of shield boards
• Antenna connector for multi-protocol wireless (BLE / Zigbee / Thread)
• 1.25MB integrated Flash and 384KB on-chip SRAM for full-featured applications and many-node wireless mesh network
PULP + VEGAboard - Driving the Ecosystem Further

• The ‘Parallel Ultra-Low Power’ (PULP) RISC-V platform
  - Prof. Luca Benini at ETH Zurich and University of Bologna
  - Open source HW approach, first released in 2016
  - 32- & 64-bit cores, peripherals, interconnect solutions in SystemVerilog
  - Single / multi-core, multi-cluster implementations

• Using VEGAboard in the University labs starting Spring 2019
  - Single versatile platform to teach both RISC-V & Arm

https://www.pulp-platform.org/
VEGAboard Early Adopter Partners

• Ashling Microsystems
• ETH Zurich
• Express Logic
• Foundries.IO
• IAR Systems
• Segger Microcontrollers Systems
OpenISA Zephyr Port on VEGAboard

**Goals**
Port RV32M1 to Zephyr RTOS. Integrate sanity tests, and provide sample applications

**Upstream**
Build RISC-V momentum around upstream software

**Vision**
Software for RISC-V must be upstream. Without this, there will be massive fragmentation

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Foundries.io
Demo: Sensor to Cloud with RISC-V

Voice commands are used to retrieve sensor data, and change light state over a low power cellular network.
Building the Future of Connected Devices

Easy to develop and prototype connected RISC-V devices utilizing the Foundries.io microPlatforms

OpenISA
VEGAboard

WNC-M14A2A

RISC-V
Zephyr™
LTE-M
AT&T
Door lock using BLUETOOTH LOW ENERGY

Control directly from BLE enabled phone

Use VEGAboard platform

Use RV32M1 SDK and implement Bare metal firmware for Smart Lock

Run firmware and BLE stack on RISC-V Zero_Riscy core

RSSI-based Auto Lock and Unlock

Manual Lock and Unlock

Smart Phone Apps

SMART LOCK APPLICATION
Wireless
  • BLE
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