Forward-Looking Statements

Safe Harbor | Disclaimers

This presentation contains forward-looking statements that involve risks and uncertainties, including, but not limited to, statements regarding our contributions to and proposals for the RISC-V ecosystem, technology and product development, business strategies and growth opportunities, the capabilities and features of our RISC-V cores, expectations regarding data growth and its drivers, and industry trends. Forward-looking statements should not be read as a guarantee of future performance or results, and will not necessarily be accurate indications of the times at, or by, which such performance or results will be achieved, if at all. Forward-looking statements are subject to risks and uncertainties that could cause actual performance or results to differ materially from those expressed in or suggested by the forward-looking statements.

Key risks and uncertainties include volatility in global economic conditions; business conditions and growth in the storage ecosystem; unexpected advances in competing technologies; our development and introduction of products based on new technologies and expansion into new data storage markets; the impact of competitive products and pricing; actions by competitors; risks associated with acquisitions, mergers and joint ventures; difficulties or delays in manufacturing; and other risks and uncertainties listed in the company’s filings with the Securities and Exchange Commission (the “SEC”) and available on the SEC’s website at www.sec.gov, including our most recently filed periodic report, to which your attention is directed. We do not undertake any obligation to publicly update or revise any forward-looking statement, whether as a result of new information, future developments or otherwise, except as required by law.
Diverse and Connected Data Types

Tight coupling between Big Data and Fast Data

**Big Data**
- Data Aggregation
- Batch Analytics
- Modeling
- Artificial Intelligence

**Fast Data**
- Streaming Analytics
- Machine Learning

**Scale**
- Insight
- Prediction
- Prescription

**Performance**
- Mobility
- Real-time Results
- Smart Machines
Innovating from the Core to Edge
Big Data & Fast Data from the Core to Edge

Big Data

- INSIGHT
- PREDICTION
- PRESCRIPTION

Scale
- core
- regional
- local

Fast Data

- MOBILITY
- REAL-TIME RESULTS
- SMART MACHINES

Latency
- remote
- edge
From General Purpose to Purpose Built

Architectures require open standard interfaces

Big Data

Expanding applications and workloads

Fast Data

General purpose compute-centric architecture

Solutions

Systems

Platforms

Devices
Western Digital RISC-V History

Motivated by our desire for open standard interfaces

2014
- uP vendors start solving general purpose problems with proprietary interfaces

2015
- Joins as platinum founding member

2016
- Explore RISC-V data centric solutions

2017
- Broadcast plan to transition to RISC-V
- Announce 1B cores

2018
- Contribute to ecosystem with Fedora Linux & Arduino Cinco ports

TODAY
To create purpose-built architectures

Harness the power of openness with RISC-V to unleash innovation

Leverage the configurability of RISC-V to ensure open standard interfaces
Western Digital Proposes Open Standard Interface for Memory Fabric – OmniXtend™

Data is the center of the architecture
No established hierarchy – CPU doesn’t ‘own’ the GPU or the Memory
Preserved Cache Coherency over the Network
Cache Coherency

Enables multiple processors to share the same memory
Coherency ensures that the processors and data are in sync
Let’s standardize a Cache Coherency Fabric

Join the collaboration

• Routable and switchable fabric
• Leverages ubiquitous Ethernet

OmniXtend initial specification at [https://github.com/westerndigitalcorporation/omnixtend](https://github.com/westerndigitalcorporation/omnixtend)
Let’s Build an Ecosystem

Join us and adopt OmniXtend as an open standard interface for new innovations with Coherent Memory Fabric Architectures
Western Digital ships in excess of 1 Billion cores per year...and we expect to double that

Transitioning our product portfolio to RISC-V over time
Introducing Western Digital’s RISC-V Core

- 2-way, superscalar, in-order core with 9 stages pipeline:
  - Support for RV32IMC
- Performance targets @ 28nm:
  - Up to 1.8 GHz operation
- Programmable Interrupt Controller
  - Supports up to 255
- AHB-lite, AXI bus options
- Verilator Clean
- RISC-V Debug support
Introducing Western Digital’s RISC-V Core

**SWERV Core Complex**

**SWERV Core – RV32IMC**

- IFU
- EXU
- DEC
- LSU

**Buses**

- LSU Bus Master
- IFU Bus Master
- Debug Bus Master
- DMA Slave Port

**Bus Options**

- 64 bit AXI, AHB-lite

**Supports**

- DCCM
- ICCM
- Icache
- PIC
- Debug
- DMA Slave

- 2-way, superscalar, in-order core with 9 stages pipeline:
  - Support for RV32IMC

- Performance targets @ 28nm:
  - Up to 1.8 GHz operation

- Programmable Interrupt Controller
  - Supports up to 255

- AHB-lite, AXI bus options

- Verilator Clean

- RISC-V Debug support
The **In Order** SweRV Core simulated tested performance was measured at 4.90

<table>
<thead>
<tr>
<th></th>
<th>Out of order</th>
<th>In order</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel Xeon E5 (Sandy)</td>
<td>7.36</td>
<td></td>
</tr>
<tr>
<td>Intel Xeon E5 (Ivy)</td>
<td>5.60</td>
<td></td>
</tr>
<tr>
<td>ARM Cortex A15</td>
<td>4.72</td>
<td></td>
</tr>
<tr>
<td>BOOM-4w</td>
<td>4.70</td>
<td></td>
</tr>
<tr>
<td>BOOM-2w</td>
<td>3.91</td>
<td></td>
</tr>
<tr>
<td>ARM Cortex A9</td>
<td>3.71</td>
<td></td>
</tr>
<tr>
<td>MIPS 74K</td>
<td>2.50</td>
<td></td>
</tr>
<tr>
<td>Rocket (RV64G)</td>
<td>2.32</td>
<td></td>
</tr>
<tr>
<td>ARM Cortex A5</td>
<td>2.13</td>
<td></td>
</tr>
</tbody>
</table>

CoreMark data from C.Celio, D.Patterson, K.Asanovic,https://www2.eecs.berkeley.edu/Pubs/TechRpts/2015/EECS-2015-167.pdf

1Estimated simulation performance based on internal Western Digital results; NOT actual comparison to CoreMark testing results
Western Digital RISC-V SweRV Core

We said our cores would be embedded and for internal use only

And ...

IT WILL BE OPEN SOURCED!

Download it CY Q1 2019:
https://github.com/westerndigitalcorporation/swerv
Western Digital SweRV Instruction Set Simulator (ISS)

We are also Open Sourcing SweRV ISS™!!!

• Implemented independently of RTL
• Models closely coupled memories, interrupt and debug
• Provides infrastructure for
  – Design verification
  – Performance modeling
• Configurable
  – Memory size
  – Instruction, Data Caches, CSRs
SweRV ISS Full Test Bench Support

• Designed to work with RTL verification
• External events are modeled
  – Checks interrupts, bus errors, etc.
• Test bench compares state change after each instruction

Download it now at: https://github.com/westerndigitalcorporation/swerv-ISS
Summary

**OmniXtend**
Cache Coherent Fabric
Open Standard
Based on Ubiquitous Ethernet

**SweRV Core**
Western Digital’s first
RISC-V designed core
Will be open sourced

**SweRV ISS**
Western Digital designed
Instruction Set Simulator
Is open sourced now

**CALL TO ACTION**
- Adopt OmniXtend & help build an open cache coherent fabric.
- Download SweRV Core and SweRV ISS. Collaborate and contribute to their development. Invest in the RISC-V ecosystem.

**INDUSTRY IMPACT**
Driving open standard interfaces and new levels of collaboration for the next generation of innovation

©2018 Western Digital Corporation or its affiliates. All rights reserved.
Creating environments for data to thrive