SiFive Core Designer

From Custom CPU to Hello World in 30 Minutes

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Silicon at the speed of software.

Design RISC-V CPUs in an hour. Get custom SoCs in weeks, not months. Impossible? Not anymore.

Start Designing
SiFive Core Designer

Your interface to SiFive RISC-V Core IP

- All SiFive Core IP is configured and delivered via the SiFive Core Designer Web Portal
  - Simple, Easy to Use, Web Interface

- Release Candidates are generated with a click of a button and available from the Workspace

- Release Candidates contain
  - RTL matching the configuration, including a testbench, and other collateral needed to realize the design
  - Documentation specific to the design
  - Customized bare-metal BSP for easy integration into SiFive’s SDKs
  - FPGA bitstreams for common FPGA development boards for easy software benchmarking of the RC
## SiFive RISC-V Core IP

### E Cores
- **32-bit embedded cores**
  - MCU, edge computing, AI, IoT
  - **E7 Series**
    - E76: Quad-core 32-bit embedded processor
    - E76-MC: Quad-core 32-bit embedded processor
    - E7: High performance 32-bit embedded core

### S Cores
- **64-bit embedded cores**
  - Storage, AR/VR, machine learning
  - **S7 Series**
    - S76: High-performance 64-bit embedded core
    - S76-MC: Multi-core: four U74 cores and one S76 core

### U Cores
- **64-bit application cores**
  - Linux, datacenter, network baseband
  - **U7 Series**
    - U74: High performance Linux-capable processor

### Series Descriptions
- **7 Series**
  - Highest performance:
    - 8-stage, dual-issue superscalar pipeline
  - **E7 Series**
    - E76-MC: Quad-core 32-bit embedded processor
    - E76: Quad-core 32-bit embedded processor
    - E7: High performance 32-bit embedded core
  - **S7 Series**
    - S76: High-performance 64-bit embedded core
    - S76-MC: Multi-core: four U74 cores and one S76 core

- **3/5 Series**
  - Efficient performance:
    - 5–6-stage, single-issue pipeline
  - **E3 Series**
    - E34: E31 features + single-precision floating point
    - E31: Balanced performance and efficiency
  - **S5 Series**
    - S54: S51 features + single-precision floating point
    - S51: Low-power 64-bit MCU core

- **2 Series**
  - Power & area optimized:
    - 2–3-stage, single-issue pipeline
  - **E2 Series**
    - E24: E21 + single-precision floating point
    - E21: E20 + User Mode, Atomics, Multiply, TIM
    - E20: Our smallest, most efficient core
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**Step 1**
Configure a custom SiFive RISC-V Core using SiFive Core Designer

**Step 2**
Use the FPGA bitstream from Step 1 to program a Digilent Arty FPGA board with the configured CPU

**Step 3**
Use Freedom Studio and the SiFive SDK to program and run Hello World
Step 1 - Configure the Core using SiFive Core Designer
Vastly customizable core IP.

Get best-in-class core IP developed by the inventors of RISC-V and customize it to your exact specifications.

Design Core
Configure a SiFive RISC-V CPU

SiFive Core Designer

- **Web Interface to Configure SiFive Core IP**
  - No Complex EDA tools or scripting languages to learn

- **What is configurable**
  - ISA, Performance levels, Modes, Ports, Interrupts, Security, Debug, and much more!

- **What is the output**
  - Verilog RTL and supporting collateral, an FPGA bitstream, software, and documentation
Core Designer UI Walkthrough

Go to the SiFive website and click “Start Designing”
  •  https://www.sifive.com/

Choose a Core Series to start from
  •  Start from a pre-configured Standard Core
  •  Or start from scratch

Name the Design and Start Clicking!
  •  Change performance levels, memory maps, Privilege modes, Instructions Sets, Security, Debug, etc...

Click Review and then Build
  •  Launches SiFive’s cloud based infrastructure to render and verify the design

Download from your SiFive Workspace
Too Many Choices? Start with a Standard Core

E3 Series

FPGA Evaluations

RTL Evaluations

E31 Standard Core Definition

Benchmarks

FE310 Silicon

Standard Core RTL and FPGA Evaluations are Available with a click-through License
Step 2 - Download the Deliverables and Program the FPGA
Download the Deliverables from your SCD Workspace
Deploy the bitstream to the FPGA

1. **Purchase a Digilent Arty**
   
   [https://store.digilentinc.com/arty-a7-artix-7-fpga-development-board-for-makers-and-hobbyists/](https://store.digilentinc.com/arty-a7-artix-7-fpga-development-board-for-makers-and-hobbyists/)

1. **Download Xilinx Vivado 2018.3 (Warning, HUGE 19GB)**
   

1. **Open Vivado’s Hardware Manager Tool**
Deploy the bitstream to the FPGA In Pictures
Coming Soon
The ability to flash Arty boards directly from Freedom Studio
Step 3 - Hello World!
Download Freedom Studio

- Freedom Studio is an Eclipse based IDE with
  - pre-built GCC and OpenOCD
  - Bundled examples for SiFive targets

- Download Freedom Studio
  - Unzip to the desired installation directory

- Or... Skip the IDE
  - Download pre-built binaries of GCC and OpenOCD from the same webpage
  - Use Freedom-E-SDK to build and debug your software using a makefile CLI based flow
    - https://github.com/sifive/freedom-e-sdk
Build and Run the Software

- File - Import - DevKit Examples - Browse
  - Select the zip that matches your core
  - Select the desired examples and click Finish
- Control-B will build the entire workspace
  - Run - Debug - OpenOCD starts a JTAG Debug Session and Loads the program