RISC-V ISA & Foundation Overview

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RISC-V Ecosystem Growth
RISC-V Summit Dec 2018

- over 1000 registered attendees
- ~2X the attendance of the Milpitas Workshop in Dec 2017
- ~250 abstracts submitted
- 59 sessions including keynotes, tutorials and 3 tracks
- 29 exhibitors
RISC-V Foundation Growth History
September 2015 to February 2019

Platinum  Gold  Silver  Auditor  Individual
Foundation: 200+ Members
So what’s all the fuss about?

It's just an ISA right?

How did we get here?
RISC-V Background

- In 2010, after many years and many projects using MIPS, SPARC, and x86 as basis of research, the Computer Science team at UC Berkeley to look at what ISAs to use for their next set of projects
- Obvious choices: x86 and ARM
  - x86 impossible – too complex, IP issues
  - ARM mostly impossible – complex, IP issues
- So UC Berkeley started “3-month project” during the summer of 2010 to develop their own clean-slate ISA
RISC-V Background (cont’d)

- Four years later, in May of 2014, UC Berkeley released frozen base user spec
  - many tapeouts and several research publications along the way
- The name RISC-V (pronounced risk-five), was chosen to represent the fifth major RISC ISA design effort at UC Berkeley
  - RISC-I, RISC-II, SOAR, and SPUR were the first four projects with the original RISC-I publications dating back to 1981
- In August 2015, articles of incorporation were filed to create a non-profit RISC-V Foundation to govern the ISA
Most CPU chips are SoCs with many ISAs

- Applications processor
- Graphics processors
- Image processors
- Radio DSPs
- Audio DSPs
- Security processors
- Power-management processor
- ....

- Apps processor ISA too large for base accelerator ISA
- IP bought from different places, each proprietary ISA
- Home-grown ISA cores
- Over a dozen ISAs on some SoCs – each with unique software stack
Why so Many ISAs?

Do we need all these different ISAs?

Must they be proprietary?

What if there was one free and open ISA everyone could use for everything?
What’s Different about RISC-V?

- **Simple**
  - Far smaller than other commercial ISAs

- **Clean-slate design**
  - Clear separation between user and privileged ISA
  - Avoids microarchitecture or technology-dependent features

- A **modular ISA**
  - Small standard base ISA
  - Multiple standard extensions

- Designed for **extensibility/specialization**
  - Variable-length instruction encoding
  - Vast opcode space available for instruction-set extensions

- **Stable**
  - Base and standard extensions are frozen
  - Additions via optional extensions, not new versions

February 2019

RISC-V Foundation
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- Incorporated August, 2015 as a 501c6 non-profit Foundation
- Membership Agreement & Bylaws ratified December 2016
- The RISC-V ISA and related standards shall remain open and license-free to all parties
  - RISC-V ISA specifications shall always be publicly available as an online download
- The compliance test suites shall always be publicly available as a source code download
- To protect the standard, only members (with commercial RISC-V products) of the Foundation in good standing can use “RISC-V” and associated trademarks, and only for devices that pass the tests in the open-source compliance suites maintained by the Foundation
The Board of Directors consists of seven+ members, whose replacements are elected by the membership.
The Board can amend the By-Laws of the RISC-V foundation via a two-thirds affirmative vote.
The Board appoints chairs of ad-hoc committees to address issues concerning RISC-V, and has the final vote of approval of the recommendation of the ad-hoc committees.
- Technical Committee Chair – Yunsup Lee, SiFive
- Security Standing Committer Chair - Helena Handschuh, Rambus
- Marketing Committee Chair – Ted Marena, Western Digital

All members of committees must be members of the RISC-V Foundation.
RISC-V Foundation Board of Directors

- Krste Asanović, Chairman
  - Professor in the EECS Department at UC Berkeley
- David Patterson, Vice-Chairman
  - Google Architect, Retired Professor Computer Science UC Berkeley
- Zvonimir Bandić, Treasurer
  - Senior Director of Next Generation Platform Technologies at Western Digital Corporation
- Charlie Hauck
  - CEO of Bluespec Inc.
- Rob Oshana
  - Director Global SW Development at NXP
- Frans Sijstermans
  - Vice President Engineering at NVIDIA
- Ted Speers
  - Technical Fellow, Head of Product Architecture for Microchip / Microsemi
The free and open RISC-V ISA is enabling a new innovation frontier across all computing devices.

Strong Industry Support
- ~200+ members; Broad commercial and academic interest

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