Linux on RISC-V

Fedora and Firmware Status Update

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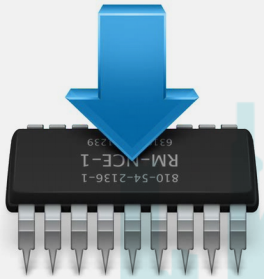
13th March 2019

RISC-V Workshop Taiwan

AGENDA



- **Status: updates for Fedora on RISC-V**
  - History: the Fedora bootstraps for RISC-V
  - Status: Fedora 29/30 on RV64GC
  - Facility: Koji status update
  - Supported Targets
- **Goal: Industry standard RISC-V server/PC**
  - Goal: make RISC-V machine BORING
  - Key components status update
- **Acknowledgments**

Status:
updates for Fedora on RISC-V

redhat.

History: The Fedora bootstraps for RISC-V

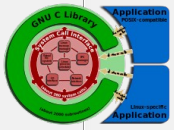
Since Fedora has an **upstream first policy**, and it also applies to Fedora/RISC-V.
We need all the key patchsets for toolchain, Linux kernel and **glibc** to be merged,
then we can do the final bootstrap on RISC-V.

rpmbuild on RISC-V

August 10, 2016

The **1st** bootstrap for **Fedora 25** as first **trial**.

October 15, 2016



Dec , 2017

The **2nd** bootstrap for **Fedora 27** as final ***preparation***

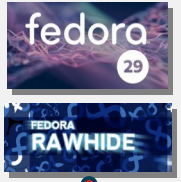
Jan 29 , 2018

The **3rd** bootstrap for **Fedora 28** was **DONE**

March , 2018

April 15, 2018

Aug , 2018



March , 2019

Status: Fedora 29/30 on RV64

Active projects:

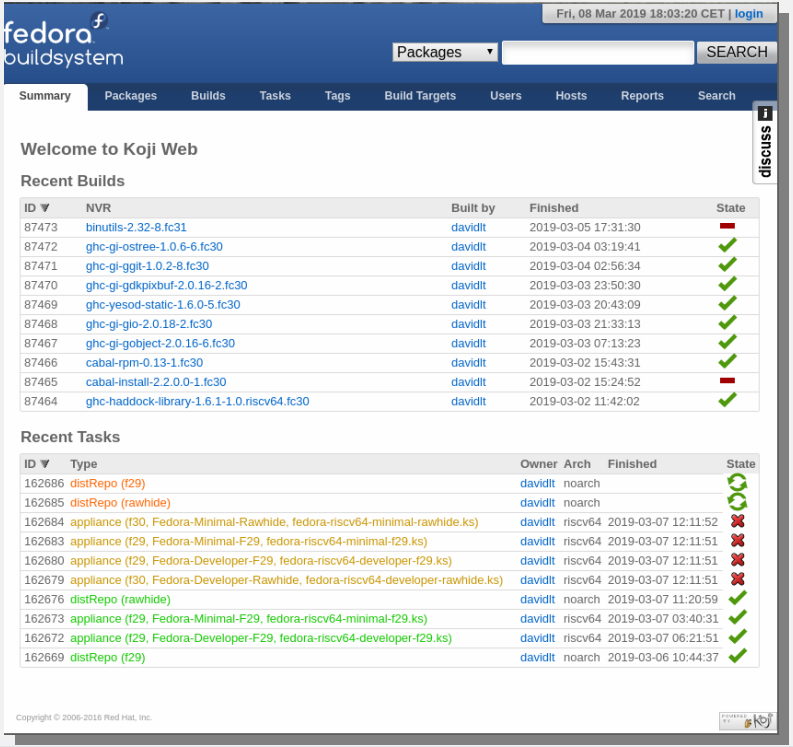
- **Fedora 29**
- **Fedora 30/Rawhide.**

Fedora for RISC-V is mirrored as a **Fedora "alternative" Architecture**, and we have some mirrored repositories:

- https://dl.fedoraproject.org/pub/alt/risc-v/
- https://mirror.math.princeton.edu/pub/alt/risc-v/

The Packages(including debuginfo, debugsource and source packages) are building in the Koji build system.

Facility: Koji system/build farm



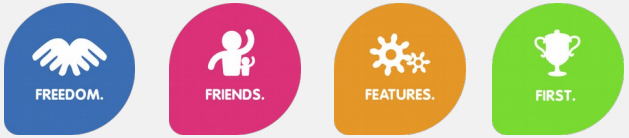
Current Hosts in build farm:

- **3 HiFive Unleasheds**
  (one with SSD)
- **64 QEMU VM**s(on x86_64):
  - fedora-riscv-x.gcc1xx.osuosl.org[2]
  - managed by libvirt
- **3** x86_64 servers for all central infrastructure of the Koji system[1]
  - 2 * Main sever and repository creation
  - 1 * VM with Ceph for backup (restic based)

[1] provided by tranquillity.se, please access: http://fedora.riscv.rocks/koji/
[2] provided by Facebook, hosted by OSUOSL and managed by GCC Compile Farm

Building 4 types of disk image:

- "**Fedora Developer**", which has extra packages installed for developers, all common editors, X11, a few small WMs, RPM tools, building tools, koji stuff, etc.
- "**Fedora Minimal**", just include @core, @buildsys-build, kernel.
- "**Fedora Nano**", smaller than Minimal, @core, kernel and no docs
- "**Fedora GNOME**", which is **Developer** with GNOME desktop GUI support.
  - For now, It can run on SiFive Unleashed with Expansion Board & PCI-E graphic Card.



Only **Developer** and **Minimal** are scheduled automatically.

Supported Targets (Virtual)

- **QEMU**: official releases work
- **libvirt/QEMU**: official releases work

Now Fedora can run on the QEMU with graphics parameters (VGA and bochs-display).

Supported Targets (Hardware)

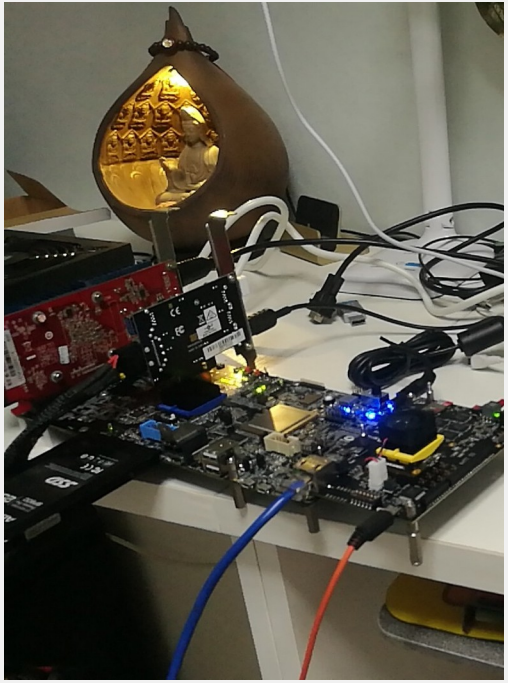
SiFive Unleashed

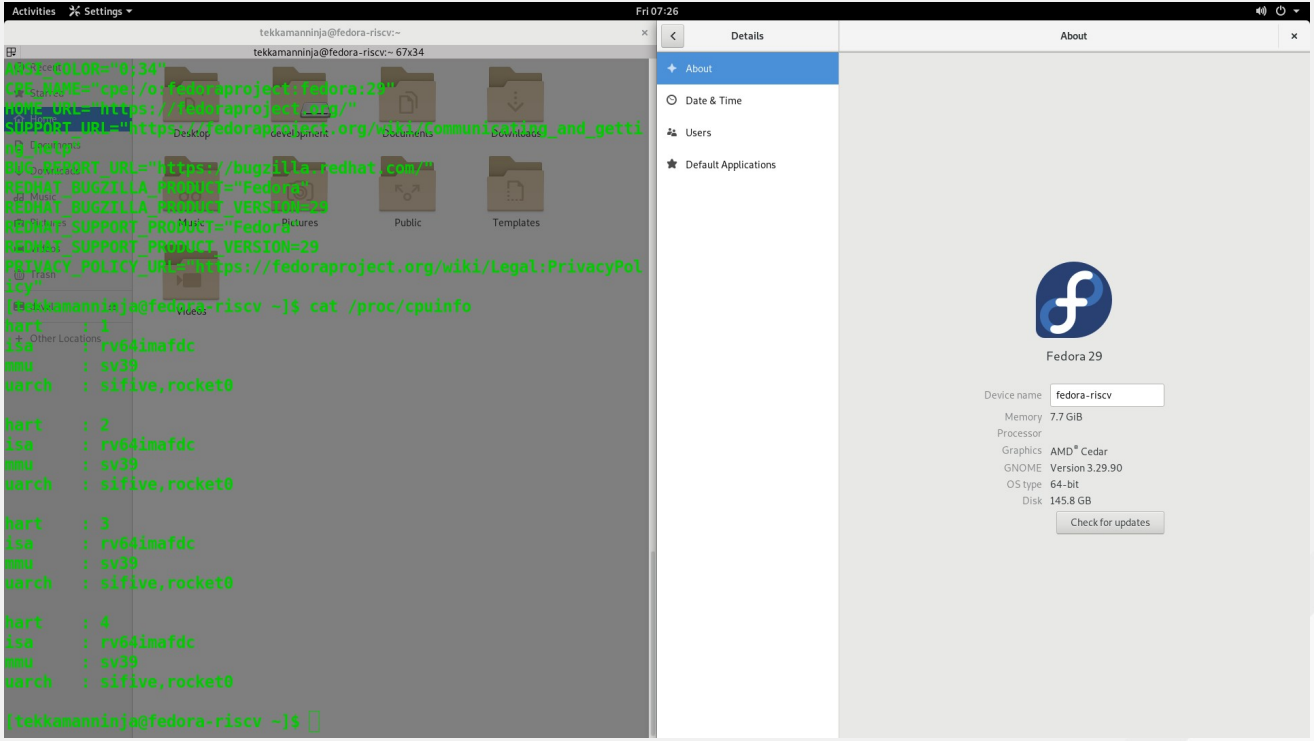
(with Expansion Board and PCI-E graphic Card)

upstream kernel lacks support, so custom kernel build is required(not included in the latest disk images).

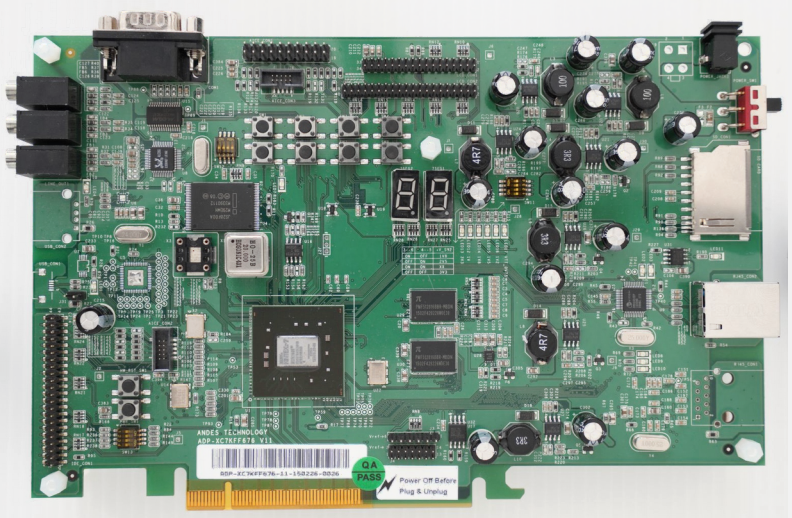
“Fedora GNOME” on SiFive Unleashed

with Expansion Board and PCI-E graphic Card





Fedora on AndeStar V5



QEMU for AndeStar V5 [1]
AndeShape Development Platform ADP-XC7KFF676

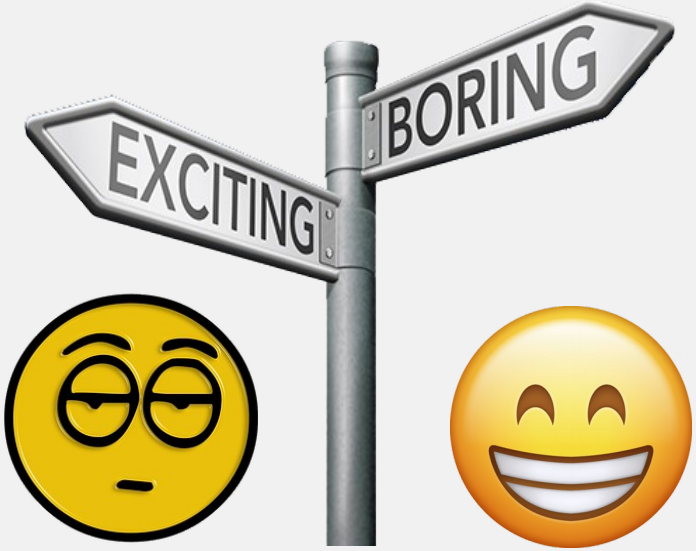
Need one little patch for mainline kernel,so haven’t been included in the latest disk images temporarily.

Fedora on RISC-V

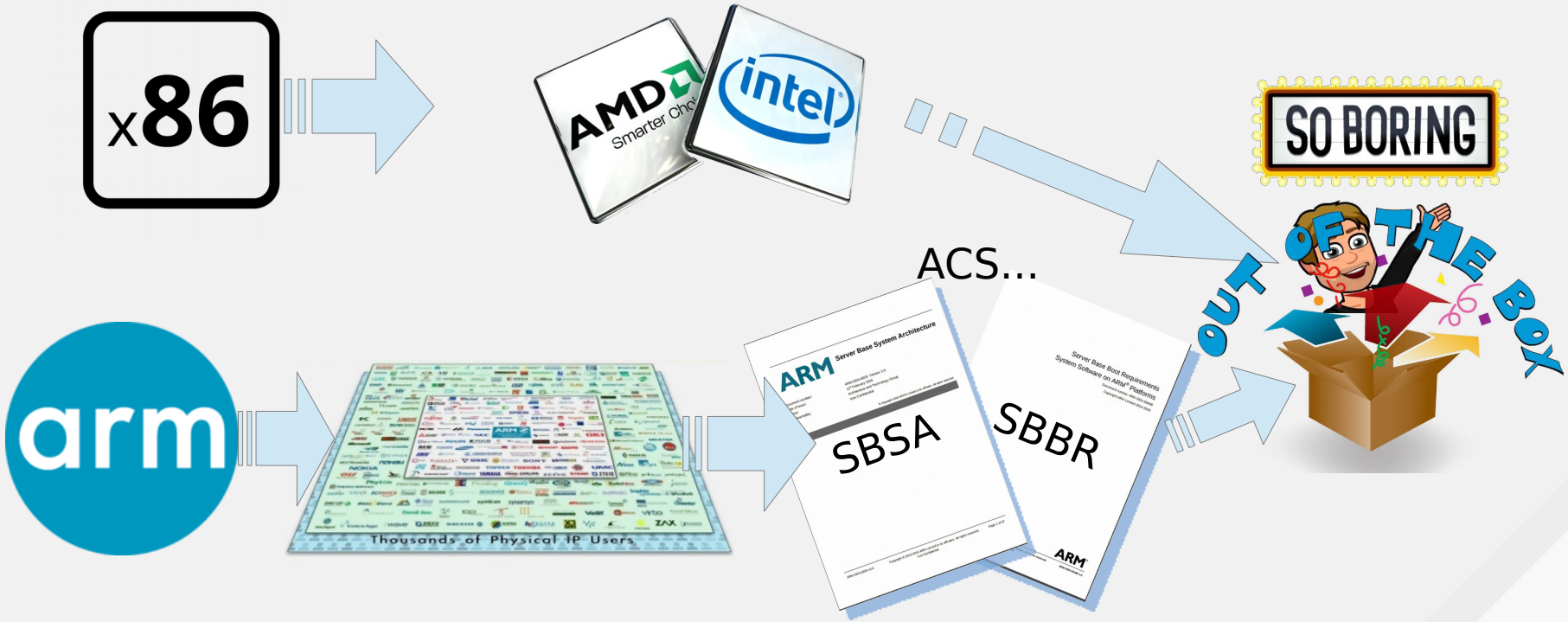
From www.codasip.com

Goal:
Industry standard RISC-V PC/server

Goal: make RISC-V machine BORING



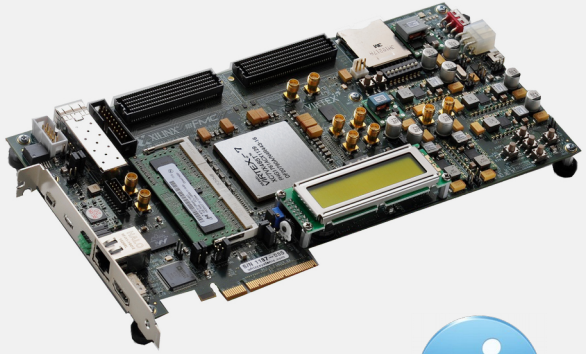
Learn from other architectures



Firmware: UEFI

(Open source Implementation: EDK2)

UEFI: Unified Extensible Firmware Interface. Firmware interface between the platform and the operating system. Major interfaces are boot services (**BS**) and run-time (**RT**) services.



HPE engineers have made some good progress on it. HPE successfully booted Tianocore EDK2 on SiFive Freedom U500 VC707 FPGA Dev Kit(with USB3.0 and PCIe 3.0 support).

Currently, it can boot into EFI Shell through remote console, but cannot load the Linux kernel yet.
HPE engineers is working on standardizing UEFI spec and RISC-V EDK2 implementation in order to conform with a variety of RISC-V platforms.

SMBIOS

- **SMBIOS Type 44, Processor Additional Information**:
  Provide SMBIOS tables for booting system to non-ACPI compliant OSes and UEFI applications on variant RISC-V processor architecture agnostic.
  - **Already proposed to DMTF SMBIOS WG, currently is in ballot process.**
  - Expect to get approval in middle of March and published in SMBIOS specification **v3.3.0**

- **RISC-V specific SMBIOS type 44 is published on RISC-V Github.**
  - https://github.com/riscv/riscv-smbios
  - currently set to private, will turn it to public, once we get the approval from SMBIOS working group.

https://www.dmtf.org/standards/smbios

CIM

Common Information Model, DMTF

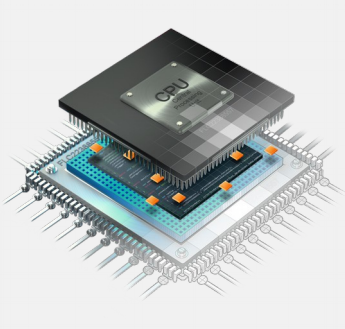
This provides a common definition of management information for systems, networks, application and services, and allows for vendor extension.

We proposed processor related CIM schema changes for RISC-V processor. The CIM changes request was approved and will be published in CIM schema v2.52.0

https://www.dmtf.org/standards/cim

Embedded Firmware:

U-boot:
The patchset for enabling RISC-V in the u-boot has been merged.



“**OpenSBI + U-Boot + Linux**” works, please check Atish Patra’s presentation
“The future of Supervisor Binary Interface(SBI)” on FOSDEM.

The GRUB2 patchset from Alexander Graf is merged. But we still miss the EFI support in kernel (so called EFI stub kernel)

Firmware

ACPI

Advanced Configuration and Power Interface

Static tables provided by system firmware to the standard ACPI compliant OS for system info and configuration, include primary run-time interpreted control methods, power management error handling and RISC-V processor architecture agnostic.

- ***MADT**, Multiple APIC Description Table:*
  Standardize Platform Level Interrupt Controller in ACPI spec.

- ***SDEI**, Software Delegated Exception Interface:*
  Provides a mechanism for registering and servicing system events from system firmware.

Redfish, DMTF

Standard API designed to deliver simple and secure management for converged, hybrid IT and the Software Defined Data Center (SDDC).

Propose Redfish schema changes for RISC-V processors.

https://www.dmtf.org/standards/redfish

PCI UEFI Expansion ROM

RISC-V PCI UEFI Expansion ROM (Code type 3):

Some PCI card require PCI expansion ROM to initialize PCI device during pre-OS system POST, such as VGA, storage, etc. PCI devices. Therefore RISC-V port of UEFI driver for PCI card is required.

Firmware proposal: OpenSBI

For OpenSBI on UEFI implementation:

- Register Supervisor mode handler to handle Machine mode interrupt for hardware events.
- Transit privilege mode
- Platform-level NV storage R/W
- OpenSBI OEM table provides OEM proprietary functionality before/or after OpenSBI platform code
- More...

Firmware proposal: UEFI

For UEFI:

- Enable pre-OS UEFI environment to execute EFI drivers in different processor privilege levels and protect the critical hardware, memory, CSR in order to mitigate malicious EFI application or driver attacks.

(This also for some emerging technologies such as Gen-Z system firmware)

For integrating RISC-V OpenSBI implementation to EDK2:

1) Integrate entire OpenSBI tree into EDK2 RiscVPkg package, utilize EDK2 custom build to build OpenSBI Library
2) Use external reference to build OpenSBI platform code from EDK2 Platform tree

HPE engineers are working on these Industrial spec change and EDK2 implementation:

Abner Chang <abner.chang@hpe.com>
HPS SW/FW Technologist

Gilbert Chen <gilbert.chen@hpe.com>
Firmware Developer

Acknowledgments

Alphabetical Listing by Company Name

facebook

David Abdurachmanov

GCC Compile Farm

Hewlett Packard Enterprise

Abner Chang

OSL OPEN SOURCE LAB

Academic Computer Club Umeå University

Al Stone
Andrea Bolognani
DJ Delorie
John Feeney
Richard Jones

ANDES TECHNOLOGY

SiFive

RISC-V

Ted Speers

TRANQUILLITY

WD

Atish Kumar Patra

redhat.

redhat.

THANK YOU

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