Segmentation Extension Proposal

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Outline

- Why segmentation
- Segmentation hardware
- New instructions
- Benefits of segmentation
- Misc
Why Segmentation

- Segmentation can be used to create multiple protection domains on a single address space
  - SASOS: Single Address Space Operating System
  - Reduce context switch overhead
  - Data sharing is easy among processes
  - ...

- Other benefits
  - I/O segment
  - Physical memory segment
  - Software-managed TLB
Segmentation Hardware

capability table

memory

p₀

p₁
Segmentation Hardware (2)
# Segmentation Hardware (3)

<table>
<thead>
<tr>
<th>segment registers</th>
<th>capability table</th>
<th>segment descriptor table</th>
<th>segment registers</th>
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<td>s0</td>
<td>data</td>
<td>perms</td>
<td>gen</td>
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<tr>
<td>s1</td>
<td>index</td>
<td>ctr</td>
<td>base</td>
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<tr>
<td>s2</td>
<td>stack</td>
<td>perms</td>
<td>gen</td>
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<td>s3</td>
<td>code</td>
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<td>s4</td>
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<td>s5</td>
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user kernel str base length
Segmentation Hardware (4)

- Segment TLB
  - Cache segment descriptors
- Segment shadow register
  - Cache capability

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New Instructions

- Load/Store with segment override
  - LW x1, \textit{s1}:imm[x2]
- Load/Store segment registers, ctr register and str register
  - LSR s0, imm[x1], SSR s0, imm[x1]
  - LCTR imm[x1], LSTR imm[x1]
- Far function call and return
  - For shared library
  - Far call
  - SJAL link\_addr, \textit{callee\_seg}, imm
Benefits of Segmentation

- On systems without paging
  - Segmentation can be used instead of PMP (Physical Memory Protection).
  - It’s more easy to implement shared library with segmentation.
Benefits of Segmentation (2)

- On systems with paging
  - I/O segment
    - No page TLB entry is needed for device driver to access its hardware device.
    - One set of load/store instructions can be used to load/store from/to either memory or I/O.
Benefits of Segmentation (3)

- On systems with paging
  - Physical memory segment
    - Improve the performance of big-memory workloads
Benefits of Segmentation (4)

- **Software-managed TLB**
  - **Prerequisite**
    - Segment/page TLB miss can not happen during TLB miss handling.
  - **How**
    - Make kernel's code, data and stack segment as physical memory segment.
    - Make kernel's code, data and stack segment descriptors always resident in segment TLB.
Misc.

- Stack growth direction
  - Stack should grow upwards.
Misc. (2)

- Compiler support is needed.
  - Far code/data pointer
  - Shared library

- OS change is needed.
  - MASOS → SASOS
Thanks.