New Members of AndeStar™ V5 Processor IPs

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CTO and EVP
Andes Technology

2019 RISC-V Workshop Taiwan
Overview of the Talk

- Latest AndeStar™ V5 Lineup
- New: Ultra-Compact Low-Power Processor
- New: Processors with DSP/SIMD ISA
- New: Processors with Multicore Cache-Coherence
- Concluding Remarks
Andes Technology Corporation

- A 14-year-old public CPU IP company
- >150 licensees worldwide
- >1B Andes-Embedded SoC shipped in 2018

- A founding member of the RISC-V Foundation
- A major open source maintainer/contributor
- Active involved in standard extensions
  - Chair of P-extension (Packed DSP/SIMD) TG
  - Co-chair of Fast Interrupt TG
  - Preparing the Performance Tools TG
# AndeStar™ V5 Processor Lineup

<table>
<thead>
<tr>
<th>Cache-Coherent Multicores</th>
<th>A25MP&lt;sup&gt;a&lt;/sup&gt;</th>
<th>AX25MP&lt;sup&gt;a&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1/2/4 A25, L2$, L1/IO coherence</td>
<td>1/2/4 AX25, L2$, L1/IO Coherence</td>
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<th>Linux with FPU/DSP</th>
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<tr>
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<td>N25F, MMU, DSP</td>
<td>NX25F, MMU, DSP</td>
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<tr>
<th>Fast/Compact with FPU/DSP</th>
<th>N25F/D25F</th>
<th>NX25F</th>
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<tr>
<td></td>
<td>V5/32b, FPU, PMP, DSP (D25F)</td>
<td>V5/64b, FPU, PMP</td>
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<th>Slim and Efficient</th>
<th>N22</th>
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<td>V5[e]/32b, 32/16 GPR</td>
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<th>AX25MP&lt;sup&gt;a&lt;/sup&gt;</th>
<th>N22</th>
<th>D22(F)</th>
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<tbody>
<tr>
<td>5-stage, A C E, &gt;1.2GHz</td>
<td>2-stage, 800 MHz</td>
<td></td>
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**Notes:**
- A(X)25MP: available Q2/2019
- 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

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Taking RISC-V® Mainstream
## AndeStar™ V5 Processors

<table>
<thead>
<tr>
<th>Cores1</th>
<th>AndeStar™ ISA2</th>
<th>GPR bits</th>
<th>Priv. levels</th>
<th>Intr. Ctrlr</th>
<th>MMU</th>
<th>I/D$</th>
<th>ECC</th>
<th>FPU3</th>
<th>DSP (P)</th>
<th>ACE3</th>
<th>MP</th>
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<tr>
<td>N22</td>
<td>V5/V5e</td>
<td>32</td>
<td>M+U</td>
<td>CLIC</td>
<td>I</td>
<td></td>
<td></td>
<td></td>
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<td>✓</td>
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1. Common features: PMP, branch prediction, CoDense™, PowerBrake, StackSafe™
2. V5: RV*IMAC + Andes Extensions, V5e: RV*EMAC + Andes Extensions
3. ✓: included; #: separately licensable
V5: Best Extensions to RISC-V

AndeStar V5: RISC-V + Andes Extensions

- **Baseline ISA extensions:**
  - Faster memory accesses
  - Faster branches
  - More compact code on top of RV-C

- **Andes Custom Extension™ (ACE) frameworks for DSA**
  - Powerful tools
  - No CPU design experience needed

- **PLIC extension:**
  - Vectored dispatch
  - Priority-based preemption
  - Save >50% of instructions

- **Cache Support:**
  - Management operations (flush, invalidate, etc.) at the line level
  - Uncached accesses
  - Write-back and write-through

- **StackSafe™:** Stack protection mechanism
- **QuickNap™:** Fast power-down/wake-up support for caches
- **PowerBrake:** Digital power throttling
AndesCore™ 22-Series
Ultra Compact and Low Power
AndesCore 22-Series

- Ultra compact and low power
- AndeStar V5 or V5e ISA
  - RV32-[IE]MC + Andes V5 extension
- 2-stage pipeline, single-issue
- AHB-lite system bus
- WFI/WFE
- Rich baseline options:
  - PMP: up to 16 entries
  - M-mode, or M+U-mode
  - Multiplier: fast or small (1 or 17 cycles)
  - Branch prediction: static or dynamic
  - I/D Local Memory: 1KB to 512MB
  - I Cache: 1KB to 32KB; direct-map or 2-way
  - HW-handled misaligned load/store
### Rich baseline options: (cont.)

- **Core-Local Interrupt Controller (CLIC)**
  - >1000 sources, 255 priority levels
  - Selective vectoring with priority preemption
  - Efficient SW-based tail chaining

- **Platform-Level Interrupt Controller (PLIC)**
  - For interrupts shared among multiple cores
  - >1000 sources, 255 priorities levels

- **Additional buses for SoC flexibility:**
  - APB private peripheral port
  - Fast IO port with 1-cycle latency

- **JTAG debug module**
  - up to 8 triggers (breakpoints/watchpoints)
  - 2-wire or 4-wire support

### Advanced features under development

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**AndesCore 22-Series**

- **PLIC**
  - Interrupt Intf.

- **PMU**
  - WFI/WFE

- **Debug**
  - HW Bkpt

- **N22 uCore, PMP**

- **ACE**

- **DSP**

- **FPU**

- **ICache**

- **Mul/Div**

- **Br. Pred**

- **ILM**

- **BIU**

- **DLM**

- **SRAM/AHBL**

- **AHBL/APB/FIO**

- **SRAM/AHBL**

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**Taking RISC-V® Mainstream**
# N22 Performance

## At 28nm
- Highest frequency (worst case): up to 800MHz
- Minimal gate count: <15K gates
- Best scores: 3.95 Coremark/MHz, 1.80 DMIPS/MHz (no-inline)

<table>
<thead>
<tr>
<th>CPU Cores</th>
<th>CPU A</th>
<th>N22 (full config)</th>
<th>CPU B</th>
<th>N22 (small config)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISA</td>
<td>V7m</td>
<td>Andes V5</td>
<td>V6m</td>
<td>Andes V5e</td>
</tr>
<tr>
<td>CoreMark/MHz</td>
<td>3.34</td>
<td>3.95 (+18%)</td>
<td>2.46</td>
<td>3.06 (24%)</td>
</tr>
<tr>
<td>DMIPS/MHz (no-inline)</td>
<td>1.25</td>
<td>1.80 (+44%)</td>
<td>0.95</td>
<td>1.46 (+54%)</td>
</tr>
<tr>
<td>CSiBE Code Size (KB)</td>
<td>1,330</td>
<td>1,185 (-13%)</td>
<td>1,315</td>
<td>1,305 (-1%)</td>
</tr>
</tbody>
</table>
AndesCore™ 25-Series
With DSP Capabilities
(D25F/A25/A25MP, AX25/AX25MP)
25-Series Overview

- **Smallest usable N25/NX25 @28nm:**
  - N25 @ 1 GHz: 37K, 4.1 uW/MHz
  - NX25@ 1 GHz: 56K, 6.0 uW/MHz

<table>
<thead>
<tr>
<th>Features</th>
<th>N*25</th>
<th>N*25F</th>
<th>A*25</th>
</tr>
</thead>
<tbody>
<tr>
<td>32KB I$/D$ + 256 BTB</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>SP/DP FPU</td>
<td>--</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>MMU and S-Mode</td>
<td>--</td>
<td>--</td>
<td>Yes</td>
</tr>
</tbody>
</table>

- **Worst-Case Freq. (GHz)**
  - N25: 1.4 GHz
  - NX25: 1.3 GHz
  - A*25: 1.2 GHz

- **Coremark/MHz**
  - N25: 3.58 (rv32), 3.52 (rv64)

- **DMIPS/MHz (no-inline)**
  - N25: 1.96 (rv32), 2.09 (rv64)

- **First implementations of P-Ext draft**

1: 28HPC+ RVT 9T library and high-speed memory. Frequency at 0.81v/-40°C.
2: BSP V5.0.0 toolchain; DMIPS/ground rule uses no-inline option.

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## Examples of DSP/SIMD Instructions

<table>
<thead>
<tr>
<th>Types</th>
<th>Instruction Operations</th>
<th>Cycles</th>
</tr>
</thead>
</table>
| **SIMD**          | Four 8x8 multiplications:  
                   16= 8x8; 16= 8x8; 16= 8x8; 16= 8x8  
                   Two 16x16 multiplications:  
                   32= 16x16; 32= 16x16                             | 1      |
| **Partial SIMD**  | Four 8x8 multiplications with 32b accumulation:  
                   32= 32 + 8x8 + 8x8 + 8x8 + 8x8 + 8x8;  
                   32= 32 + 8x8 + 8x8 + 8x8 + 8x8 + 8x8 (2<sup>nd</sup> op: RV64 only)  
                   Two 16x16 multiplications with 32b accumulation:  
                   32= 32 + 16x16 + 16x16  
                   32= 32 + 16x16 + 16x16 (2<sup>nd</sup> op: RV64 only) | 2      |
| **RV64 Only**     | Two 32x32 multiplications with 64b accumulation:  
                   64= 64 + 32x32 + 32x32                                                   | 3      |
### Speedup with P-Ext on 25-Series

#### DSP libraries for RV32-P (>200 functions in 8 categories)

<table>
<thead>
<tr>
<th>Speedup</th>
<th>Basic</th>
<th>Cmplx</th>
<th>Ctrl</th>
<th>Filter</th>
<th>Matrix</th>
<th>Ststcs</th>
<th>Xform</th>
<th>Utils</th>
<th>ALL</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVG</td>
<td>2.40</td>
<td>1.62</td>
<td>1.84</td>
<td>2.26</td>
<td>1.62</td>
<td>2.44</td>
<td>1.29</td>
<td>1.08</td>
<td>1.82</td>
</tr>
<tr>
<td>MAX</td>
<td>5.16</td>
<td>4.09</td>
<td>2.13</td>
<td>4.11</td>
<td>2.75</td>
<td>4.39</td>
<td>1.78</td>
<td>1.43</td>
<td>5.16</td>
</tr>
</tbody>
</table>

#### DSP libraries for RV64-P (>200 functions in 8 categories)

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<tr>
<td>AVG</td>
<td>4.73</td>
<td>1.92</td>
<td>1.31</td>
<td>2.41</td>
<td>3.04</td>
<td>4.14</td>
<td>1.28</td>
<td>1.19</td>
<td>2.50</td>
</tr>
<tr>
<td>MAX</td>
<td>10.81</td>
<td>4.14</td>
<td>1.59</td>
<td>5.04</td>
<td>6.83</td>
<td>8.51</td>
<td>1.67</td>
<td>2.72</td>
<td>10.81</td>
</tr>
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#### Speedups for various applications

<table>
<thead>
<tr>
<th>Cores</th>
<th>RV64-P</th>
<th>RV32-P</th>
</tr>
</thead>
<tbody>
<tr>
<td>APP</td>
<td>CIFAR10 (image classification)</td>
<td>PNET (90% of face detection)</td>
</tr>
<tr>
<td>Speedup</td>
<td>10.99</td>
<td>7.57</td>
</tr>
</tbody>
</table>
AndesCore™ A(X)25MP: Multicores with Cache Coherence
A(X)25MP: Cache-Coherent Multicore

AndesCore™
A25MP/AX25MP Multicore

Platform-Level Interrupt Controller

Debug Support

Bus Master Interface (AXI-128)

1~4 A25/AX25 CPUs:
- RV-IMACFD ISA + V5 extensions
- P-extension draft
- Supporting SMP Linux

Bus Interfaces
- LM slave port
- Coherence slave port
- AXI bus master interface
  - N:1 synchronous clock ratio

PLIC for interrupt handling
Debug/trace support
### A(X)25MP: Cache-Coherent Multicore

**AndesCore™ A25MP/AX25MP Multicore**

- **ACU Coherence Unit**
  - MESI cache coherence protocol
  - Duplicate L1 dcache tags
  - IO coherence for cacheless masters

- **L2$ Controller (optional)**
  - Size: 128KB to 2MB
  - Line size: 32B
  - **16-way** with pseudo random replacement and writeback

- **SRAM optimization**:
  - SRAM access cycles: ≥ 2 (configurable)
  - Bank interleaving:
    - 2 tag banks, 8 data banks
  - Fully pipelined without contention

**Components**

- **Platform-Level Interrupt Controller**
- **Debug Support**
- **ACU Engine/ L2 Cache Controller**
- **Bus Master Interface (AXI-128)**

- **IRQ’s**
- **JTAG**
- **Trace Port (x4)**
- **I/D LM Slave Port (AHB-32/64 x4)**
- **Coherence Slave Port (AXI-64)**

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A(X)25MP: Cache-Coherent Multicore

- **L2$ Controller (cont.)**
  - Writeback/invalidate control
  - **ECC protection** (SECDED): same as that for L1 memory

- **Prefetching**
  - Instruction: 1/2/3 lines after a miss
  - Data: 2/4/8 lines after consecutive linear misses (tracking 8 address sequences)

- **Linux-capable configuration**
  - RV64, 32KB I/D$, 256-entry BTB, 128-entry STLB, 8-entry PMP
  - ~1 GHz at 28nm (worst case)
  - Size (gate count):
    - Core: >200K, ACU+L2: <200K

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**AndesCore™ A25MP/AX25MP Multicore**

- **Platform-Level Interrupt Controller**
- **Debug Support**
- **ACU Engine/ L2 Cache Controller**
  
  - **A25/AX25**
    - ILM, DLM
    - I$, D$
  
  - **A25/AX25**
    - ILM, DLM
    - I$, D$

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**Bus Master Interface (AXI-128)**

- **IRQ's**
- **JTAG**
- **Trace Port (x4)**
- **I/D LM Slave Port (AHB-32/64 x4)**
- **Coherence Slave Port (AXI-64)**
Concluding Remarks

- Andes is working hard to catch up RISC-V demands

- Our offerings:
  - 22-series: ultra compact and low power cores
  - 25-series: fast and full-featured with Linux SMP supports
  - DSP ISA for the emerging needs for built-in efficient data processing
  - Andes Custom Extension™ for growing demands for DSA
  - Strong development tools and SW support from Andes and partners

- Diversified applications:
  - AI, FPGA, IoT, MCU, Security, Storage, Wireless

Andes: Trusted Computing Expert and Your Best RISC-V Partner!
Thank You !!
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