Enabling Embedded Intelligence

Jack Kang, RISC-V Workshop Taiwan 2019
SiFive Core IP
Embedding Intelligence Everywhere

**Consumer**
AR/VR/Gaming devices
Smart Home
Imaging/Wearables

**Storage/Networking/5G**
SSD, SAN, NAS
Base Stations, Small cells, APs
Switches, Smart NICs, Offload cards

**ML/Edge**
Sensor Hubs, Gateways
Autonomous machines
IoT devices
32-bit Embedded Processors

64-bit Embedded Processors

64-bit Application Processors

Intelligent Edge

Intelligent Cloud

Embedding Intelligence from the Edge to the Cloud
SiFive Core IP
2 series:

SiFive’s **smallest** and most **efficient** RISC-V processor IP
SiFive Core IP
3 and 5 series:

The world's most deployed
RISC-V processor IP

Efficient Configurable Mature
32-bit Embedded Processors

Efficient Performance Coherent, Heterogenous, Multicore Hard Real-time capabilities
64-bit Embedded Processors

Configurable Efficient Mature
64-bit Application Processors
SiFive Core IP
7 series:
The highest performance commercial RISC-V processor IP

Common Feature sets
Hard Real-time capabilities
Unprecedented scalability

~60% increase in CoreMarks/MHz*
~40% increase in DMIPS/MHz*
10% increase in Fmax*

*Compared to SiFive 5 series
Scalable throughput provided by 8+1 cores per cluster

Extensible design via custom instructions

Configurable memory architecture for application specific tuning

Tightly integrated memory for low latency access

64-bit addressability for real-time latency sensitive applications

Mixed-precision arithmetic for efficient compute of ML workloads

Enhanced determinism for hard real-time constraints

Functional safety provided by in-built fault tolerance mechanisms

A single pre-integrated and verified deliverable

Cache lock capability for mission-critical computing

In-cluster coherent heterogenous combination of real-time and application processors

SiFive 7 Series
Embedded Intelligence Everywhere
<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coherent in-cluster combination</td>
<td>of application processors and real-time processors</td>
</tr>
<tr>
<td>Configurable memory maps and coherent accelerator ports</td>
<td>for tightly coupling storage specific accelerators</td>
</tr>
<tr>
<td>Optional FPU</td>
<td>for applications which don’t need floating point capability</td>
</tr>
<tr>
<td>Tightly integrated memories and Cache lock capability</td>
<td>for critical real time workloads</td>
</tr>
<tr>
<td>Deterministic mode</td>
<td>for FAST DATA applications with hard real-time constraints</td>
</tr>
<tr>
<td>Storage, ML, Cryptography specific custom instructions</td>
<td></td>
</tr>
<tr>
<td>64-bit real-time addressability</td>
<td>for BIG DATA applications</td>
</tr>
</tbody>
</table>
## 5G/Networking

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complex arithmetic capability</td>
<td>for accelerating baseband functions</td>
</tr>
<tr>
<td>High bandwidth accelerator ports</td>
<td>for enabling intelligent offload processing</td>
</tr>
<tr>
<td>Configurable memory maps</td>
<td>for optimizing QoS</td>
</tr>
<tr>
<td>In-cluster coherence of application and real-time processor</td>
<td>enables 5G latency (&lt;1ms) requirements</td>
</tr>
<tr>
<td>Hard real-time capabilities</td>
<td>for scheduling baseband protocol layers</td>
</tr>
<tr>
<td>High throughput</td>
<td>processing for next gen 5G stacks</td>
</tr>
<tr>
<td>Tightly Integrated Memories and Cache lock capability</td>
<td>for critical real time workloads</td>
</tr>
</tbody>
</table>
### AR/VR/Sensor Fusion

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low Latency peripheral access</td>
<td>and coherent accelerator port</td>
</tr>
<tr>
<td>Coherent in-cluster combination</td>
<td>of application processors with real time processors</td>
</tr>
<tr>
<td>Simple caching hierarchy</td>
<td>for ease of application optimization</td>
</tr>
<tr>
<td>Combine with SiFive</td>
<td>2, 3 or 5 series for designs with tight power constraints</td>
</tr>
<tr>
<td>Workload specific customizations</td>
<td>(AR/VR/MR/CV)</td>
</tr>
<tr>
<td>Mixed precision arithmetic</td>
<td>for accelerating machine learning compute</td>
</tr>
</tbody>
</table>
Recently announced products

Wearable AI

Enterprise

Edge

Rapid adoption of SiFive Core IP from the Edge to the Core
SiFive Core IP: Embedding Intelligence Everywhere

- Efficient Performance
- Scalability
- Compelling Feature Set

Embedding intelligence for a world of a Trillion Connected Devices
Silicon verified. Market proven.

The most advanced configurable core IP and silicon solutions from the inventors of RISC-V.

Microcontrollers  ▶  Embedded  ▶  Linux  ▶  Multicore

▶ Networking  ▶  Storage  ▶  Computing  ▶  AI
▶ Industrial  ▶  IoT  ▶  Consumer  ▶  Automotive

www.sifive.com