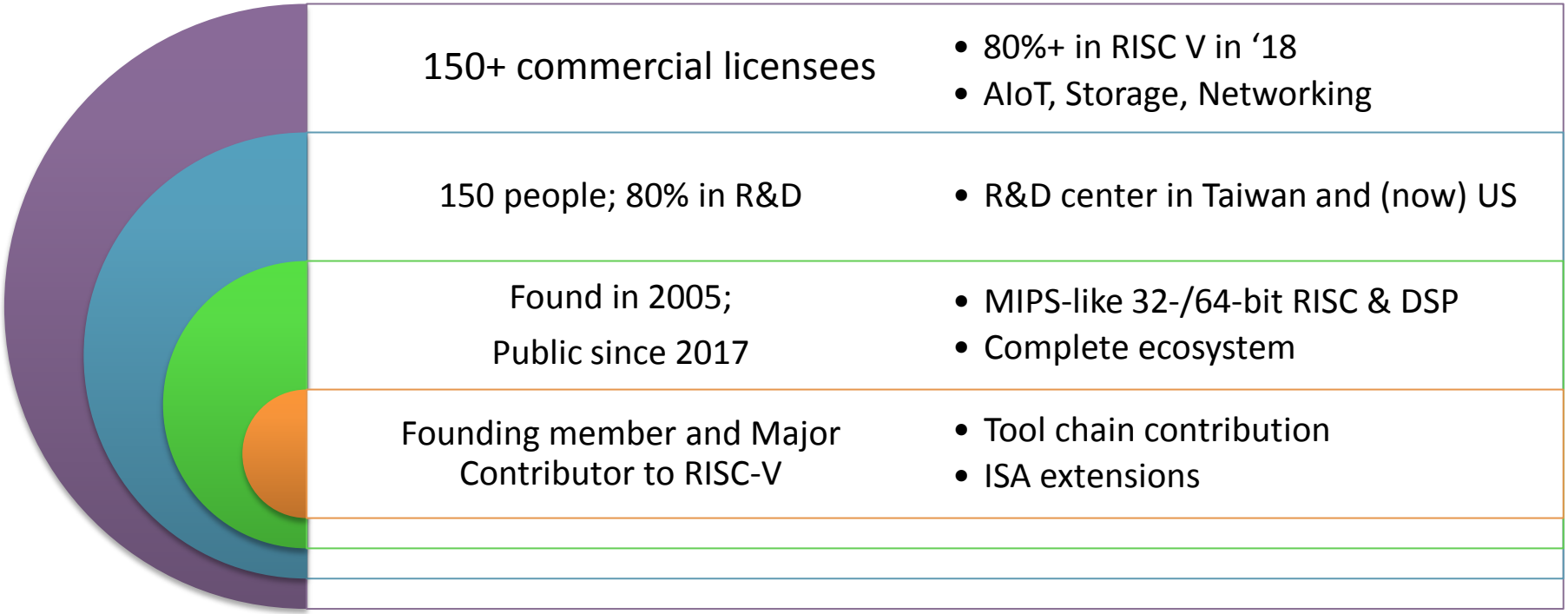
Andes Company Overview

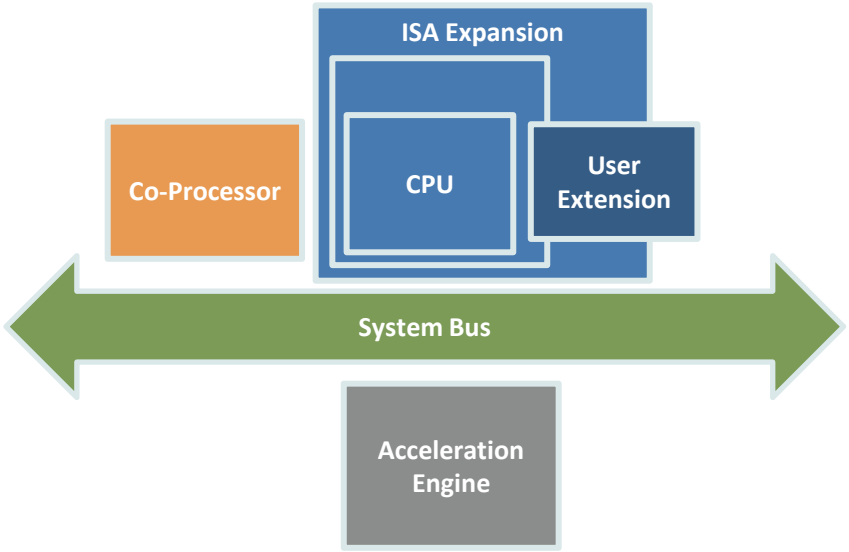
Driving Innovations™

Andes: Converting 10+ Years Investments into RISC-V Community



ANDES TECHNOLOGY

Evolution of Computing Acceleration



- Specialized peripherals
  - I/O controller, crypto engines
- Co-processors
  - Floating point (FPU)
- ISA expansion
  - Intel's MMX, SSE, AVX, etc.
- User extensions
  - Old: ARC, Tensilica
  - New: RISC-V open opcode

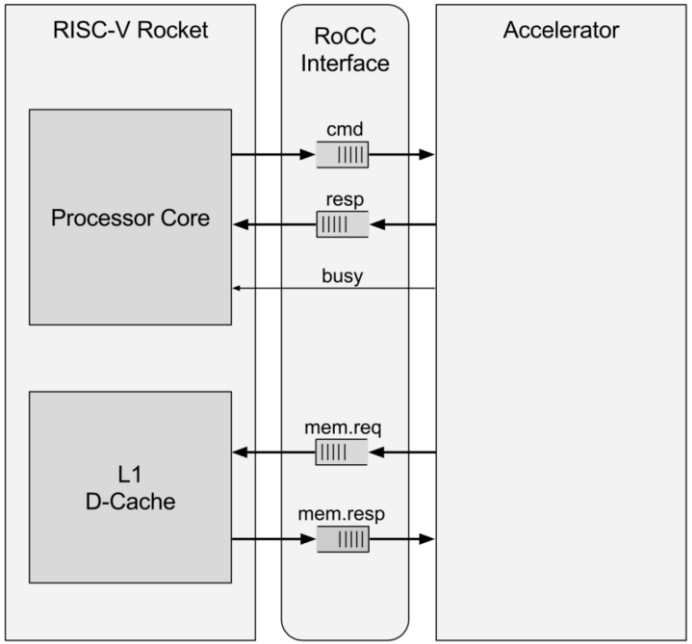
Comparison of Acceleration Methods

	Peripheral	Co-Processor	ISA Expansion	User Extension
Start-up latency	Longest	Long	None	None
Resource sharing	None	Decode/Control	Control & RF	Control & RF
Implementation Freedom	A TON	Lots	None	Restricted
Proprietary advantage	Yes	Yes	None	Yes
Best for	Very heavy Semantic	Medium Semantic	Commoditized Computation	Low-Medium Semantic

$$\frac{\text{Medium Semantic Acceleration}}{\text{Long start-up Latency}} =$$

ANDES TECHNOLOGY

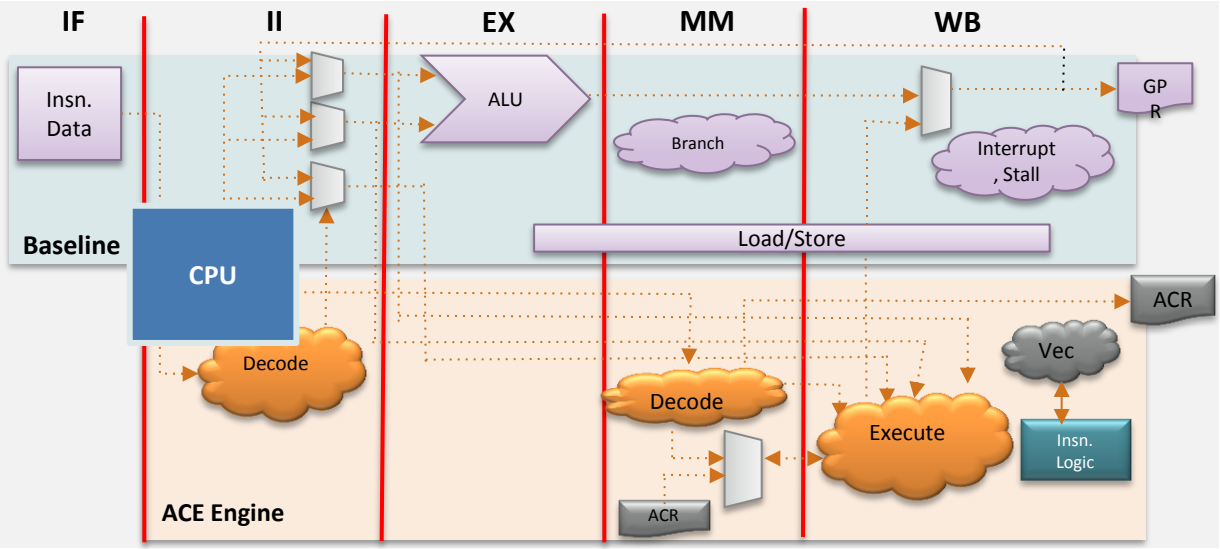
RISC-V ROCC Interface for ISA Extension



- Loosely coupled transaction model
  - Command queues starts in order
  - Response not guaranteed to be in-order
- Memory model same as baseline ISA
- Ideal for light-semantic operations
  - Custom ALU/data format
  - Dependent on host for resource/schedule

ANDES TECHNOLOGY

Andes Custom Extension (ACE) Illustrated



- RISC-V compliant 25-bit
- ACR can be arbitrarily wide
- Multiple ACMs
- Automated RISC-V to ACE signals

User-written

Auto-generated

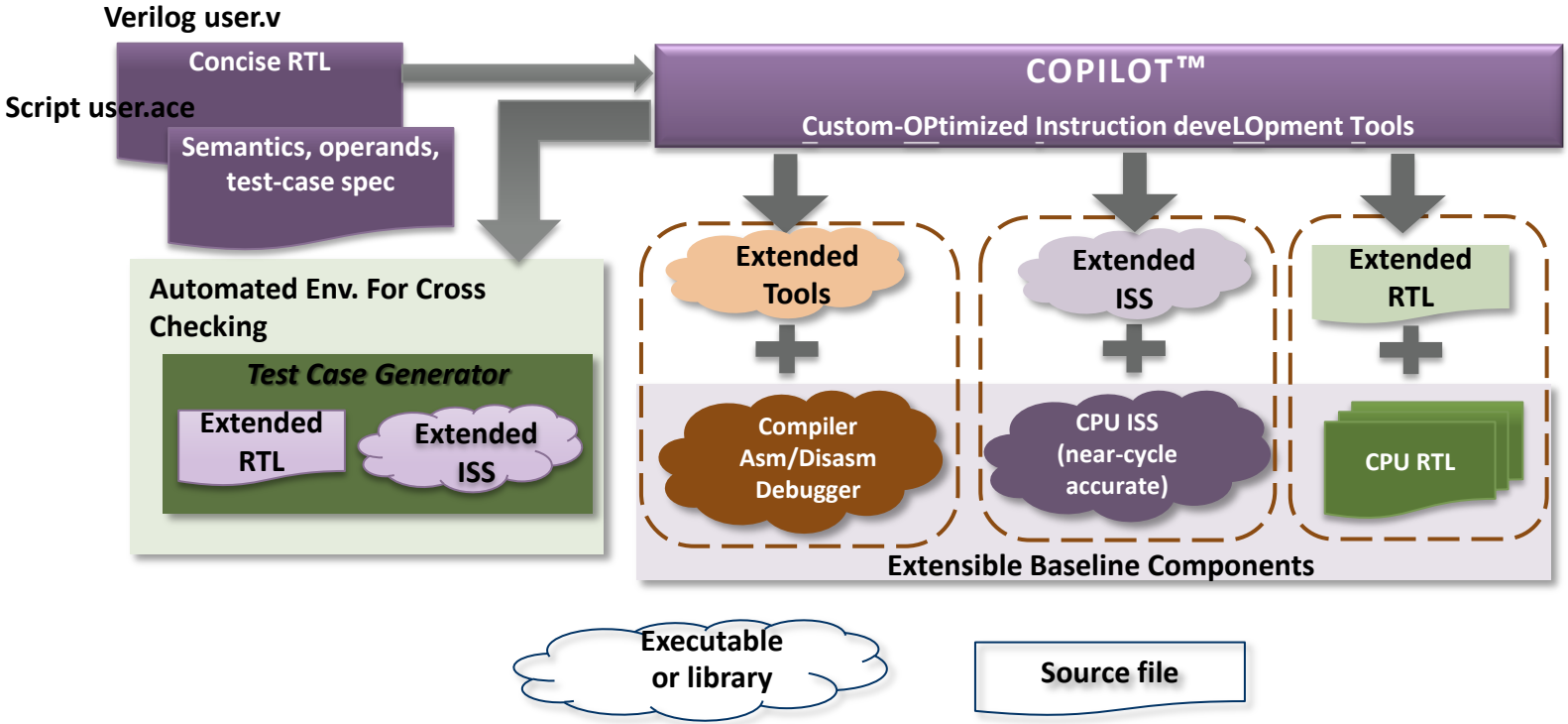
Auto-generated (IF)

ANDES TECHNOLOGY

Summary of ACE Capabilities

Items	Description	
Instructions	scalar	single-cycle, or multi-cycle
	vector	for loop, or do-while loop
	background option	retire immediately, and continue execution in the background. Applicable to scalar and vector.
Operands	standard	immediate, GPR, baseline memory (thru CPU)
	custom	- ACR (ACE Register), ACM (ACE Memory) - Arbitrary width and number - ACR operands can be “implied” to save opcode

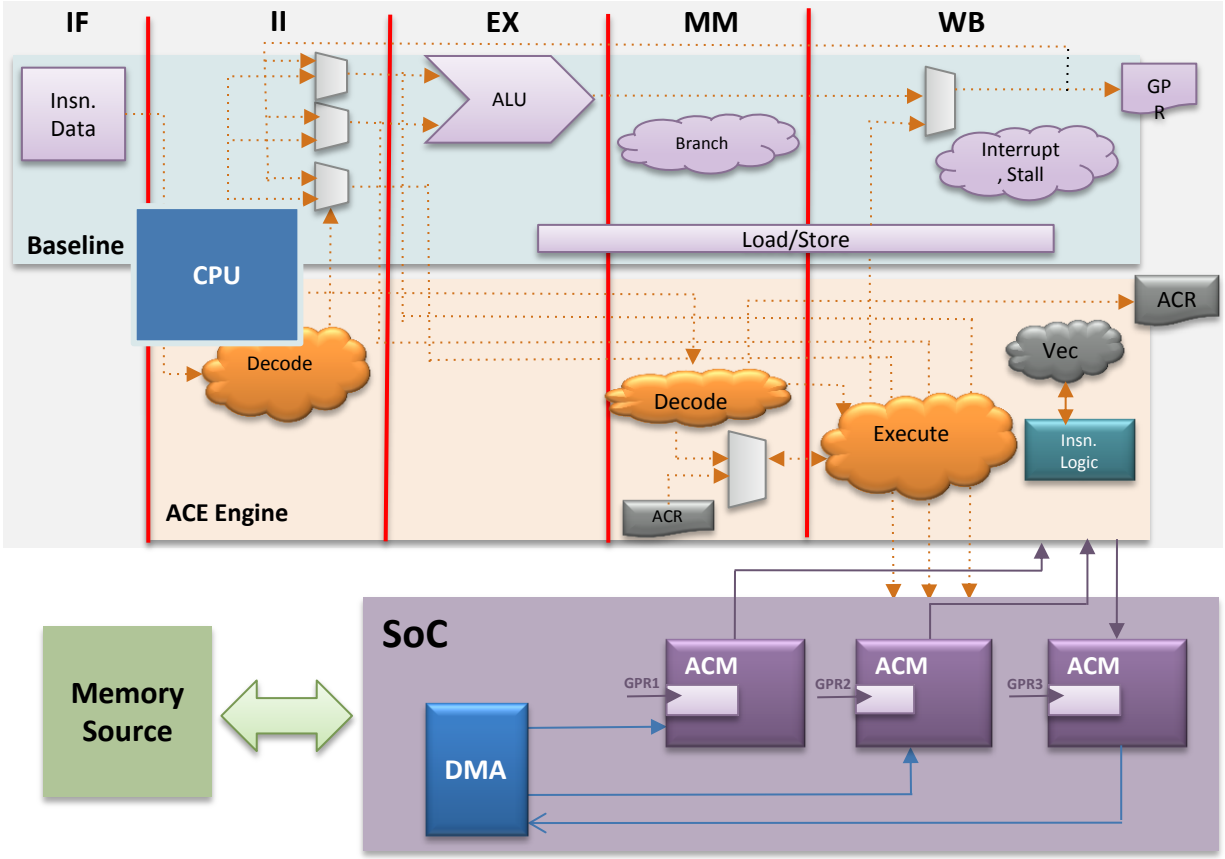
ACE and COPILOT Environment



ACE: More Capability, MUCH More Automated

Items	ROCC	Andes
Capability Low-level process signals availability	Yes	Yes ++
Assignment of opcode & operands	Manually assigned	Auto assigned
RTL to decode the instructions	Manually developed	Auto-generated
RTL to check instruction dependences	Manually developed	Auto-generated
Function verification tools, patterns and flow	Manually developed	Auto-generated
Compiler/debugger for the new instructions	Manually developed	Auto-generated
Programming with the new instructions	Inline assembly	high-level intrinsic
Support for custom registers/memory ports	No	Yes
RTL to do repeated operations on new data	Manually developed	Auto-generated

ACE Use Case in Embedded Datapath



- RISC-V calculates pointers, kick-starts DMA, coordinates systems
- ACE instructions pass GPR pointers to ACE engines
- All signals wired automatically
- All tools generated by COPILOT

User-written

Auto-generated

Auto-generated (IF)

ANDES TECHNOLOGY