RISC-V: high performance embedded SweRV™ core microarchitecture, performance and CHIPS Alliance

Ted Marena
Western Digital Corporation

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Agenda

• Introduction:
  – First superscalar, high performance, fully verified, OPEN SOURCE 32-bit RISC-V core
• SweRV core microarchitecture
• SweRV core ISS
• Performance benchmarking
• SweRV FPGA Design
• CHIPS Alliance
  – Applications and challenges
• Conclusion
SweRV Core™: Western Digital’s First RISC-V Core
SweRV – 1st Production grade open source RISC-V

- https://github.com/westerndigitalcorporation/swerv_eh1
- A lot of traffic!
SweRV Core™ Complex

- RISCV 32IMC Core
  - First internally developed RISCV core
- RISCV debug support
- Programmable Interrupt Controller
  - Support for up to 255 external interrupts
- AHB-lite, AXI bus support
- Frequency target
  - 1 GHz at SSG process corner
- Technology
  - TSMC 28 nm
SweRV Core Microarchitecture

- 9 stage pipeline
- 4 stall points
  - Fetch1
    - Cache misses, line fills
  - Align
    - Form instructions from 3 fetch buffers
  - Decode
    - Decode up to 2 instructions from 4 instruction buffers
  - Commit
    - Commit up to 2 instructions / cycle

- EX pipes
  - ALU ops statically assigned to I0, I1 pipes
  - ALU’s are symmetric

- Load/store pipe
  - Load-to-use of 2

- Multiply pipe
  - 3 cycle latency

- Divide pipe
  - 34 cycles, out-of-pipe
• Branch direction is predicted using GSHARE algorithm
  – XOR of global branch history and PC
    • Used to lookup branch direction in branch history table (BHT)
  – PC hash
    • Used to lookup branch target in branch target table (BTB)
  – The sizes of the branch target buffer (BTB) and the branch predictor table (BPT) are independently configurable with up to 512 and 2048 registers
SweRV Instruction Set Simulator I

• Open sourced: https://github.com/westerndigitalcorporation/swerv-ISS

• SweRV core ISS is a set of tools for RISC-V functional and performance testing:
  – includes load and run RISC-V executable and linkable (ELF) binaries
  – Verilog format hexadecimal memory image files

• It currently implements the RV32I instruction set with M and C extensions, and RV64I:
  – All control and status registers are implemented and it is architected with multi-hart support

• In the interactive mode, the SweRV ISS can:
  – run and debug RISC-V software
  – examine RISC-V state and memory contents
  – run in single and multiple steps
SweRV Core Physical Design

- TSMC 28 nm
  - 125 C, SVT, 150 ps clock skew

- SSG corner w/out memories
  - 1 GHZ
    - .132 mm²
  - 800 MHZ
    - .100 mm²
  - 500 MHZ
    - .093 mm²

- TT corner w/out memories
  - 1 GHZ
    - .092 mm²
  - 800 MHZ
    - .091 mm²
  - 500 MHZ
    - .088 mm²
5.0 CoreMark/MHz
- Additional performance gains are possible with compiler optimizations
- Multi-threaded/multi-core results are always renormalized to a single execution context

2.9 Dhrystone MIPs/MHz
- Using optimized strcpy function

CoreMark data from C. Celio, D. Patterson, K. Asanovic, https://www2.eecs.berkeley.edu/Pubs/TechRpts/2015/EECS-2015-167.pdf
SweRV Core Nexys4 Reference Design Overview

- SWERV Core
- AXI Fabric
- SRAM
- UART
- Xilinx Tools: Vivado, Chipscope
- Debugging Tools: OpenOCD+GDB/Lauterbach
- UART Terminal: Minicom
- FPGA
- JTAG
- Clock 
- Reset
- IFU
- LSU
- SB
- DMA
- SWERV wrapper
- DCCM
- ICCM
- ChipScope
- ILA
SweRV FPGA Prototype

• Prototype on Nexys-4 DDR board
  – Artix 7 FPGA (Xilinx part number XC7A100T-1CSG324C)
  – 128MiB DDR2
  – Quad-SPI flash

• System clock runs at 40 MHz

• Shared JTAG/UART port is primarily used to download the bit file on FPGA and UART printfs.

• Olimex CPU JTAG probe is used to download and debug application software

• We used Xilinx Vivado 2018.2 toolchain for our reference design
SweRV Core FPGA Design Information

- [https://github.com/westerndigitalcorporation/swerv_eh1_fpga](https://github.com/westerndigitalcorporation/swerv_eh1_fpga)
NAND Controller SoC applications

- Multi-purpose SoC for consumer SSD applications
- First RISC-V based SoC for NAND controller applications
- Advantages:
  - Full advantage of open source software ecosystem for RISC-V
  - Instruction optimization for NAND media handling
  - Freedom of power and performance optimization for end application
What is CHIPS Alliance?

› Organization which hosts and curates high quality, open source hardware code

› A barrier free environment for collaboration

› Shared resources which lower the cost of hardware development
Project Goals

› Leverage common hardware development efforts so
  • IP blocks can be broadly used
  • Verification contributions benefit all

› Deliver high quality, open source CPU designs, and complex IP blocks
  • Known validated blocks that can be quickly adopted
Why Join CHIPS Alliance

› Share resources to lower the cost of hardware development
› Receive high quality, open source CPU designs and complex IP blocks
› Open Source Collaboration and Diversity can now benefit hardware

See more: www.chipsalliance.org
Driving Momentum

Western Digital ships in excess of 1 Billion cores per year
...and we expect to double that.
Summary

- SweRV Core EH1 and SweRV ISS now available on Github
- SweRV Core FPGA design on Github
- Open sourced these to help accelerate the RISC-V Ecosystem
- Consider Joining CHIPS Alliance to accelerate RISC-V hardware
BACKUP