Innovation Unleashed: Solutions Enabling Embedded Intelligence

SiFive China
Agenda

01 Global Trends
02 SiFive Core IP Portfolio
03 Domain Specific Features
04 Commercial Products
05 Future
Global Trends

26% CAGR
2017 - 2022

Source: Cisco VNI Global IP Traffic Forecast, 2017 - 2022
SiFive Core IP
Embedding Intelligence Everywhere

**Consumer**
- AR/VR/Gaming devices
- Smart Home
- Imaging/Wearables

**Storage/Networking/5G**
- SSD, SAN, NAS
- Base Stations, Small cells, APs
- Switches, Smart NICs, Offload cards

**ML/Edge**
- Sensor Hubs, Gateways
- Autonomous machines
- IoT devices
Embedding Intelligence from the Edge to the Cloud

- U Cores: 64-bit Application Processors
- S Cores: 64-bit Embedded Processors
- E Cores: 32-bit Embedded Processors

Intelligent Edge
Intelligent Cloud
SiFive Core IP

2 series:

SiFive’s **smallest** and most **efficient** RISC-V processor IP

- **E2 Series**
  - 32-bit Embedded Processors
  - Higher Performance
  - Configurable
  - Low latency interrupts

- **S2 Series**
  - Tiny, Full Featured, 64-bit MCU
  - Efficient RISC-V MCU
  - Configurable Core and Memory System
  - Ultra low-latency interrupts
SiFive Core IP
3 and 5 series:
The world's most deployed RISC-V processor IP

Efficient Performance
Coherent, Heterogenous, Multicore
Hard Real-time capabilities

Configurable
Efficient
Mature
SiFive Core IP 7 series:

The highest performance commercial RISC-V processor IP

- **E7 Series**: 32-bit Embedded Processors
- **S7 Series**: 64-bit Embedded Processors
- **U7 Series**: 64-bit Application Processors

**Common Feature sets**
- Hard Real-time capabilities
- Unprecedented scalability

**Performance Improvements**
- ~60% increase in CoreMarks/MHz*
- ~40% increase in DMIPS/MHz*
- 10% increase in Fmax*

*Compared to SiFive 5 series*
## Core IP 7 Series

### Standard Cores

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<thead>
<tr>
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<tbody>
<tr>
<td>01</td>
<td>E76, E76-MC</td>
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<tr>
<td>02</td>
<td>S76, S76-MC</td>
<td></td>
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<tr>
<td>03</td>
<td>U74, U74-MC</td>
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Standard Cores represent pre-configured implementations of a Core Series which are available for free RTL and FPGA evaluations.
SiFive 7 Series
Embedded Intelligence Everywhere

Scalable throughput provided by 8+1 cores per cluster

Extensible design via custom instructions

Configurable memory architecture for application specific tuning

Tightly integrated memory for low latency access

64-bit addressability for real time latency sensitive applications

Mixed-precision arithmetic for efficient compute of ML workloads

Enhanced determinism for hard real-time constraints

Functional safety provided by in-built fault tolerance mechanisms

A single pre-integrated and verified deliverable

Cache lock capability for mission-critical computing

In-cluster coherent combination of real-time and application processors
## Product Map

### E Cores
- **32-bit embedded cores**
  - MCU, edge computing, AI, IoT

### S Cores
- **64-bit embedded cores**
  - Storage, AR/VR, machine learning

### U Cores
- **64-bit application cores**
  - Linux, datacenter, network baseband

### 7 Series
- **E7 Series**
  - **E76-MC**
    - Quad-core 32-bit embedded processor
  - **E76**
    - High performance 32-bit embedded core
- **S7 Series**
  - **S76-MC**
    - No 64-bit Cortex equivalent
  - **S76**
    - High-performance 64-bit embedded core
- **U7 Series**
  - **U74-MC**
    - Compare to Cortex-A55 MP4
  - **U74**
    - High performance Linux-capable processor

### 3/5 Series
- **E3 Series**
  - **E34**
    - E31 features + single-precision floating point
  - **E31**
    - Balanced performance and efficiency
- **S5 Series**
  - **S54**
    - No 64-bit Cortex equivalent
  - **S51**
    - Low-power 64-bit MCU core
- **U5 Series**
  - **U54-MC**
    - Compare to Cortex-A53
  - **U54**
    - Linux-capable application processor

### 2 Series
- **E2 Series**
  - **E24**
    - E21 + single-precision floating point
  - **E21**
    - E20 + User Mode, Atomics, Multiply, TIM
  - **E20**
    - Our smallest, most efficient core
- **S2 Series**
  - **S21**
    - No 64-bit Cortex equivalent
  - **S21**
    - Area-efficient 64-bit MCU core
# Storage

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<th>Feature</th>
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<tr>
<td><strong>Coherent in-cluster combination</strong> of application processors and real-time processors</td>
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<tr>
<td><strong>Deterministic mode</strong> for FAST DATA applications with hard real-time constraints</td>
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<tr>
<td><strong>Configurable memory maps and coherent accelerator ports</strong> for tightly coupling storage specific accelerators</td>
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<tr>
<td><strong>Tightly integrated memories and Cache lock capability</strong> for critical real time workloads</td>
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<tr>
<td><strong>Optional FPU</strong> for applications which don’t need floating point capability</td>
</tr>
<tr>
<td><strong>Storage, ML, Cryptography specific custom instructions</strong></td>
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<tr>
<td><strong>64-bit real-time addressability</strong> for BIG DATA applications</td>
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### 5G/Networking

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<tr>
<th>Feature</th>
<th>Description</th>
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<tbody>
<tr>
<td>Complex arithmetic capability</td>
<td>for accelerating baseband functions</td>
</tr>
<tr>
<td>High bandwidth accelerator ports</td>
<td>for enabling intelligent offload processing</td>
</tr>
<tr>
<td>Configurable memory maps</td>
<td>for optimizing QoS</td>
</tr>
<tr>
<td>Tightly Integrated Memories and Cache lock capability</td>
<td>for critical real time workloads</td>
</tr>
<tr>
<td>In-cluster coherence of application and real-time processor</td>
<td>enables 5G latency (&lt;1ms) requirements</td>
</tr>
<tr>
<td>Hard real-time capabilities</td>
<td>for scheduling baseband protocol layers</td>
</tr>
<tr>
<td>High throughput processing</td>
<td>for next gen 5G stacks</td>
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## AR/VR/Sensor Fusion

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<tr>
<td><strong>Low Latency peripheral access and coherent accelerator port</strong></td>
<td>Coherent in-cluster combination of application processors with real time processors</td>
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<tr>
<td><strong>Coherent in-cluster combination</strong> of application processors</td>
<td>Workload specific customizations (AR/VR/MR/CV)</td>
</tr>
<tr>
<td><strong>Simple caching hierarchy</strong></td>
<td>Mixed precision arithmetic for accelerating machine learning compute</td>
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<td><strong>Combine with SiFive 2, 3 or 5 series for designs with tight power constraints</strong></td>
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Enterprise SSD

- FADU Annapurna SSD Controller
  - World’s first RISC-V SSD controller
- FADU Bravo Series Enterprise SSD
- 3.5GB throughput and 800K IOPS at less than 1.8W
- Powered by SiFive E51

“SiFive’s RISC-V Core IP was 1/3 the power and 1/3 the area of competing solutions, and gave FADU the flexibility we needed in optimizing our architecture to achieve these groundbreaking products.” J. Lee, FADU CEO
Intelligent Edge

- Microsemi’s PolarFire SoC
- World’s first RISC-V SoC FPGA architecture bringing Real-time to Linux
- Targeted for real-time Linux applications at the Edge
- Defense-grade security features
  - Secure boot
  - DPA safe crypto core
  - SECDED on all memories
  - Physical memory protection/PMP
- Powered by SiFive U54-MC and SiFive E51
Wearable AI

- **Huangshan No. 1 (MHS001)** from Huami using Upbeat Tech

- **Integrated biometric signal processor** with 4 dedicated AI engines and built-in CNN based inference engine

- 38 percent more efficient than the Arm Cortex-M4

- Powered by **SiFive E31**

“The world’s first artificial intelligence powered wearable chipset”
SiFive Core IP: Embedded Intelligence Everywhere

- Efficient Performance
- Scalability
- Compelling Feature Set

Embidding intelligence for a world of a Trillion Connected Devices
• Best in class in RISC-V based solution with local customer support

• Leader in RISC-V ecosystem development to support China semiconductor industry, growing with open-source community

• Pioneer in cloud-based SaaS service for custom ASICs.

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