Introduction to Codasip and RISC-V IP

BK Series Cores
The Company
Who We Are and What We Do
Who is **Codasip**?

- The leading provider of **RISC-V** processor IP
- Founded in 2014 in the Czech Republic
  - Based on 10 years of university research on processor design automation
  - Founding member of the RISC-V Foundation, [www.riscv.org](http://www.riscv.org)
  - Now Codasip GmbH, with offices in Silicon Valley and Czech Republic
- Provides unique design automation tools for easy processor modification
  - IoT: performance/power efficiency and low-cost
  - Algorithm accelerators (DSP, security, audio, video, etc.)
  - Profiling of embedded SW for tailoring processor IP
- **Codasip Bk** = portfolio of RISC-V processors
Codasip RISC-V Solutions

- **Reduce the cost** of custom processor development
  - Automation and usage of standards enable custom processors to easily integrate into any design environment

- **Simplify** custom processor programming
  - Generate open-source tools for any processor type to deliver powerful technology that is easy to integrate

- **Enable extensible and fully custom** processor methodologies
  - Make small optimizations to proven processor IP, or implement a completely unique processor solution
BK: Customizable RISC-V Cores

- Codasip RISC-V cores are all pre-verified, tape-out quality IP
- Codasip RISC-V cores are all customizable
  - RISC-V ISA extensions for your application needs
  - Easily create new processor resources
    - Custom registers for computations
    - Custom control-status registers
    - Custom interfaces such as GPIO, FIFO, scratch-pad memory
    - Even modify the pipeline…
**BK cores Roadmap**

**Bk3, Bk5, Bk5-64, Bk7**
- Available now, 100% RISC-V compliant
- Fully customizable
- Address wide performance range

**Bk future cores**
- High-performance cores
  - Advanced pipelines
  - Comprehensive DSP features
- Most energy-efficient cores

Comprehensive offering including new advanced designs
Customization & Tools
Our Solutions for Easy RISC-V Customization
Codasip Studio

Studio = unique collection of tools for fast & easy modification of RISC-V processors. All-in-one, highly automated. Introduced in 2014, silicon-proven by major vendors.

Customization of base instruction set:
- Single cycle MAC
- Custom crypto functions
- And many more…

Complete IP package on output:
- C/C++ LLVM-based compiler
- C/C++ Libraries
- Assembler, disassembler, linker
- ISS (incl. cycle accurate), debugger, profiler
- UVM SystemVerilog testbench

CodAL – processor description language

```
element i_mac {
  use reg as dst, src1, src2;
  assembly { "mac" dst "," src1 "," src2 }
  binary { OP_MAC dst src1 src2 0:bit[9] }
  semantics {
    rf[dst] += rf[src1] * rf[src2];
  }
};
```

Integrated processor development environment

RTL Automation
- Verilog
- VHDL

SDK automation

Verification Automation

C/C++ LLVM-based compiler
- C/C++ Libraries
- Assembler, disassembler, linker
- ISS (incl. cycle accurate), debugger, profiler
- UVM SystemVerilog testbench

Codasip GmbH
Bk Core Customization with Codasip Studio

Codasip Studio automatically generates all processor IP design kits and verifies for RISC-V compliance (you still need to verify your own resources and instructions).

Start from Bk3/5/7 cores
1. Add instructions
2. Add resources
3. Modify pipeline
4. …

Your RISC-V CodAL Models

Your RISC-V HDK
- RTL models
- Synthesis scripts
- Verification models and simulators
- Virtual prototypes

Hardware Design Kit

Your RISC-V SDK
- Compiler
- Assembler
- Linker
- Debugger
- IDE etc

Software Design Kit

Codasip Studio Toolset

Profiling of embedded application SW enables processor optimizations

ISA extensions are quickly implemented and analyzed during design space exploration
RISC-V offers a wide range of ISA modules:

- I/E for integer instructions
- M for multiplication and division
- C for compact instruction
- F/D for floating point operations
- WIP: B, P, V, …

However, it may not be enough for your application domain or if you are looking for a key differentiator…

RISC-V allows custom extensions

SDK must be aware of the custom extensions

High level of automation needed

Codasip has tools for this task: Codasip Studio
ISA Customization Benefits

- ISA customization achieves PPA optimization
  - **Performance**: Efficient ISA will reduce the number of instructions for tasks.
  - **Power**: Efficient ISA will reduce total cycle counts thus reducing MHz.
  - **Area**: Efficient ISA can reduce code size and data size (table) so that total area (logic and memory) becomes smaller, too.

- ISA customization can be your differentiator…
  …while keeping vast majority of ecosystem benefits.
Example: B Extension Functional Model

- Written in CodAL
  - In 10 days by a single engineer
- 900 LOC
- SDK with C compiler, ISS and profiler to check the impact of the extensions is automatically generated by Studio
  - Compiler can use a subset of instructions automatically (rotations, compact instructions, shifts, etc.)

```c
element i_zip
{
    use opc_zip as opc;
    use reg any as dst, src1;
    use shift_imm as imm;
    assembler { opc dst "," src1 "," imm};
    semantics
    {
        rf_gpr_write (dst, gzip_uXlen(rf_gpr_read(src1), imm));
    };
    set isa_b := i_zip;
}
```

```c
uxlen gzip_uXlen (const uxlen rsrc1 , const uxlen mode)
{
    uint32 zip_mode, x ;
    x = rsrc1;
    zip_mode = mode & 31;
    if(zip_mode & 1)
    {
        if(zip_mode & 2)
            x = gzip_stage (x, MASK_ZIP2_L, MASK_ZIP2_R, 1);
        if(zip_mode & 4)
            x = gzip_stage (x, MASK_ZIP4_L, MASK_ZIP4_R, 2);
        if(zip_mode & 8)
            x = gzip_stage (x, MASK_ZIP8_L, MASK_ZIP8_R, 3);
        if(zip_mode & 16)
            x = gzip_stage (x, MASK_ZIP16_L, MASK_ZIP16_R, 4);
    }
    return x;
}
```
Example: B Extension Implementation Model

- Written in CodAL
  - In 3 weeks by a single engineer
- 1500 LOC
- Hardware design kit (HDK) with RTL, testbench and UVM based verification environment automatically generated by Studio

```c
#define OPTION_EXTENSION_B
    case SLO:
        ex_result = ones_shifter_32(SLO, ex_aluop1, ex_aluop2);
        break;
    case SRO:
        ex_result = ones_shifter_32(SRO, ex_aluop1, ex_aluop2);
        break;
    case ANDC:
        ex_result = (uxlen)ex_aluop1 & (~ ex_aluop2);
        break;
    case ROTP:
        ex_result = ex_aluop1 >> ex_aluop2;
        break;
    case ROTL:
        ex_result = ex_aluop1 << ex_aluop2;
        break;
    case CTZ:
        ex_result = codasip_ctlz_uint32(ex_aluop1);
        break;
    case CLZ:
        ex_result = codasip_cttz_uint32(ex_aluop1);
        break;
#endif
```
Why Customization-Aware SDK?

One of the biggest advantages of the RISC-V open ISA is customization. However, a customized processor also needs a customized SDK…

Standard customization (manually adding custom ISA extensions):

1. Model and simulate a new instruction
2. Modify the compiler
3. Modify assembler
4. Add support in the debugger
5. Verify, verify, verify…

→ Challenging, time-consuming, expensive

Benefits of automatic generation of a customized LLVM compiler:

✔ Reduced time needed for compiler modification
✔ Reduced cost of custom processor development
✔ The resultant processor will be easily programmable using standard C/C++
✔ Proven open-source LLVM framework allows for easy integration
CodeSpace: Eclipse-based IDE

- Based on LLVM compiler and debugger
- SDK management
  - You can change the SDK for a software project with just a few clicks
- Profiler perspective
  - Integration with profiler tools directly with editors
- Enhanced debugging perspective
  - You can view ports, signals, or pipeline
- On-chip debugging
  - You can move from ISS to on-chip debugging within the same environment with the same software project
Customer Successes

Our Customers and How We Helped Them
Vidtoo Technology

Selected product(s):

- Bk3 processor
  - RISC-V-based, fully configurable and extensible
  - Single 3-stage in-order execution processor pipeline
  - Optional caches, IEEE 1149.1 debug, industry-standard bus interfaces

Customer will use it for:

- High-performance computing (HPC) chips

“After careful consideration, we determined that Codasip offered the best combination of performance, value and design expansion ability. Those traits, plus best-in-class support and the broad ecosystem that the open RISC-V ISA brings, gave us confidence that Codasip was the right choice.”

Thomas Hu, CEO of Vidtoo Technologies

Hangzhou, China

Leader in semiconductor products for HPC (high-performance computing), artificial intelligence and machine learning platforms:

- Inference engines for data centers
- 3D video processing technologies for industrial IoT applications
- SR (Simulated Reality)/MR (Mixed Reality) applications with on-chip decision-making capabilities
Mythic

Selected product(s):

• Bk3 processor
  - RISC-V-based, fully configurable and extensible
  - Single 3-stage in-order execution processor pipeline
  - Optional caches, IEEE 1149.1 debug, branch prediction, industry-standard bus interfaces

• Codasip Studio
  - Complete toolset for automated optimization and modification of RISC-V cores

Customer will use it for:

• Neural networking chips

“Codasip gave us the flexibility to create a truly unique RISC-V processor, specific to our needs. This saved us the effort to build our own processor from scratch and allowed us to focus on other critical areas of the product development.”

Ty Garibay, VP of Hardware Engineering at Mythic

Redwood City, California
Austin, Texas

Leader in artificial intelligence (AI) computing technology based on a unique approach to neural network processing. Mythic’s powerful, yet energy-efficient life-enhancing AI solutions can be pushed into anything, from fitness bands and hearing aids to self-driving cars and security cameras.
Dongwoon Anatech

Selected product(s):

- Bk3 processor
  - RISC-V-based, fully configurable and extensible
  - Single 3-stage in-order execution processor pipeline
  - Optional caches, IEEE 1149.1 debug, industry-standard bus interfaces

Customer will use it for:

- Motor control IC products

“The RISC-V instruction set with custom DSP extensions delivers the performance we require while keeping silicon area to a minimum. The best-in-class Codasip Studio development tools enable us to profile our software and find an optimal set of instructions for our application.”

Jin Park, CTO of Dongwoon Anatech

Seoul, Korea

Leader in analog and power ICs (integrated circuits) for mobile phones. Analog product portfolio includes:

- Auto-focus driver IC for smartphones
- AMOLED DC-DC converter
- Display power driver IC
- Haptic driver IC
Trinamic

Selected product(s):

- Bk3 processor
  - RISC-V-based, fully configurable and extensible
  - Single 3-stage in-order execution processor pipeline
  - Optional caches, IEEE 1149.1 debug, industry-standard bus interfaces
- Codasip Studio
  - Complete toolset for automated optimization and modification of RISC-V processors

Customer will use it for:

- Next generation of motion microcontroller product series

“We opted for RISC-V because the open ISA ensures the longevity our customers require. Among alternatives, Codasip’s Bk3 offered the ideal combination of performance and power efficiency that our applications demand.”

Jonas P. Proeger, Marketing Director of Trinamic
Summary

- Codasip provides comprehensive RISC-V IP, from 32bit embedded to 64bit Linux-ready RISC-V cores
  - Fully verified, complete IP packages
    - No need to obtain 3rd party packages to start
    - No need to verify IP
  - Full-time customer support staff

- **Codasip Studio** enables RISC-V optimization
  - Unique in the industry