OpenHW Group

Proven Processor IP

Corporate & CORE-V Overview

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OPENHW GROUP™
PROVEN PROCESSOR IP

Outline

- OpenHW Group & CORE-V family launched
- What problem are we addressing?
- OpenHW Group Purpose & Structure
- Initial Working Groups & Task Groups
- CORE-V Demos

OPENHW GROUP™ PROVEN PROCESSOR IP and CORE-V™

- **OpenHW Group** is a not-for-profit, global organization driven by its members and individual contributors where hardware and software designers collaborate in the development of open-source cores, related IP, tools and software such as the CORE-V Family of cores. OpenHW provides an infrastructure for hosting high quality open-source HW developments in line with industry best practices.

- **CORE-V** is a series of RISC-V based open-source cores with associated processor subsystem IP, tools and software for electronic system designers. The CORE-V family provides quality core IP in line with industry best practices. The IP is available in both silicon and FPGA optimized implementations. These cores can be used to facilitate rapid design innovation and ensure effective manufacturability of high-volume production SoCs.

Strong multi-national partners

CORE-V™

Community

RISC-V®

ECLIPSE FOUNDATION

FOSSi Foundation

Marketing

publitek marketing communications

Accounting, Legal, Banking

pwc

NORTON ROSE FULBRIGHT

RBC

OpenHW Group Initial Sponsors

OpenHW Group Board of Directors

Five to seven board directors

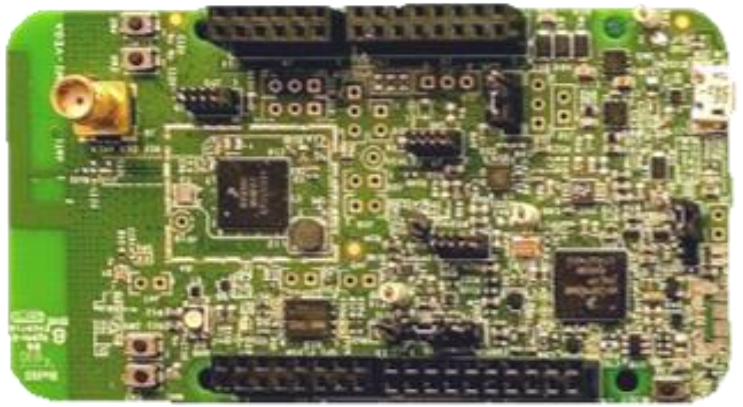
- Initial BoD appointed with staggered term
- Replacements elected by membership

  - Rob Oshana, NXP (Chairman)
  - Charlie Hauck, Bluespec (Treasurer)
  - Alessandro Piovaccari, Silicon Labs
  - Xiaoning Qi, Alibaba Group
  - Rick O'Connor, OpenHW Group

NXP and OPENHW GROUP PROVEN PROCESSOR IP

CORE-V

- Why does NXP participate in the OpenHW Group?
  - Facilitates rapid innovation
  - Research and education collaboration with world class universities such as ETH Zurich
  - Accelerates ecosystem expansion and support
  - Successful adoption of PULP technology for Vega program and internal development
  - “Community” as well as “Commercial” distros (to use a Linux analogy) lead to a robust ecosystem



VEGA

PULP Parallel Ultra Low Power

www.open-isa.org

OpenHW Group Status

- Legally registered open source, not-for-profit corporation
- OpenHW Group & CORE-V family launched June 6th, 2019
  - Visit www.openhwgroup.org for further details
- Follow us on Social media
  - Twitter @openhwgroup
  - LinkedIn OpenHW Group
- Strong supporting testimonials from 17 sponsors & partners
- OpenHW Group corporate governance, by-laws, IP rules, membership drafting well underway
- Join our sponsor group to influence how to this important open source hardware initiative takes shape

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SoC Development Cost Drivers

- Software, RTL design, Verification and Physical design account for ~90% of overall SoC development costs
- For highly differentiated IP blocks and functions, this investment is warranted
- For general purpose CPU cores an effective open-source model can drive down these development costs and increase re-use across the industry

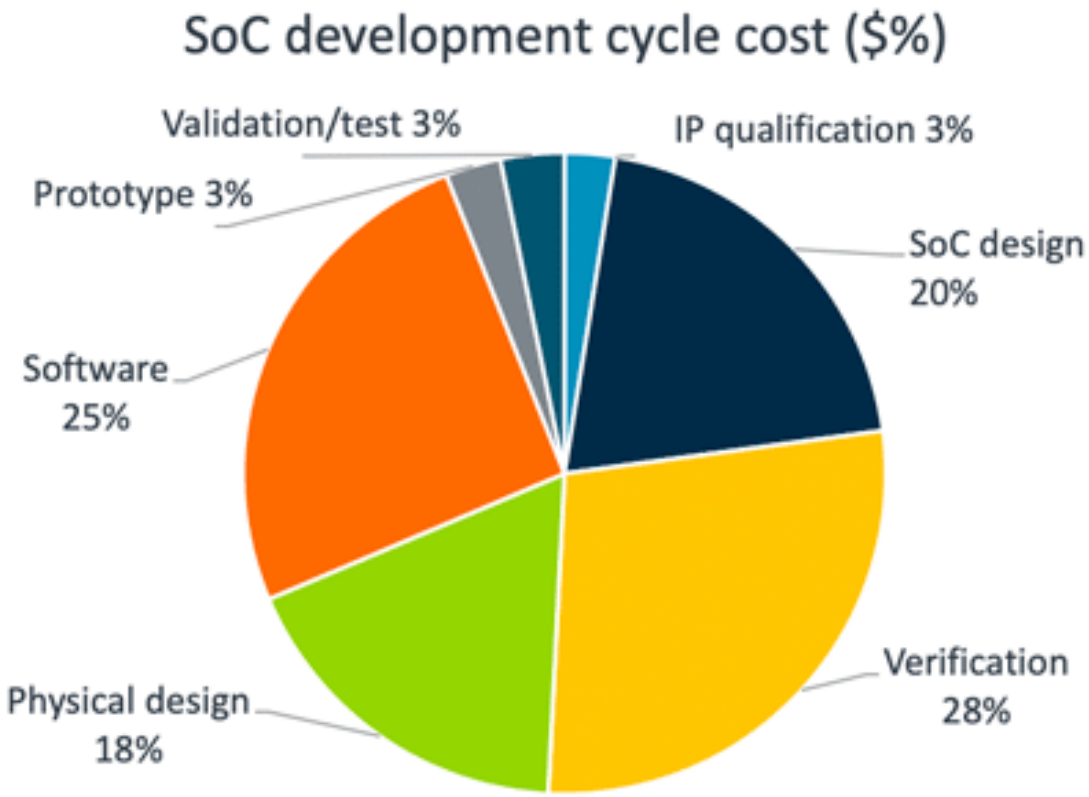

Image Source: Arm Ecosystem Blog

RISC-V ISA Brings Open Source Paradigm to CPU Design

- The free and open RISC-V ISA unleashes a new frontier of processor design and innovation
- How many open source processor implementations do we need as an industry?
  - Open cores are great from a pedagogical teaching perspective, but how many is too many for widespread industry adoption?
- How does the industry, ecosystem, community organize to ensure open core success?
  - How do we establish critical mass around a handful of open cores?

Many RISC-V Open Source Cores… …and counting….

(source: riscv.org)

Name	Maintainer	Links	User spec	License
rocket	SiFive, UCB Bar	GitHub	2.3-draft	BSD
freedom	SiFive	GitHub	2.3-draft	BSD
Berkeley Out-of-Order Machine (BOOM)	Esperanto, UCB Bar	GitHub	2.3-draft	BSD
ORCA	VectorBlox	GitHub	RV32IM	BSD
RI5CY	ETH Zurich, Università di Bologna	GitHub	RV32IMC	Solderpad Hardware License v. 0.51
Zero-riscy	ETH Zurich, Università di Bologna	GitHub	RV32IMC	Solderpad Hardware License v. 0.51
Ariane	ETH Zurich, Università di Bologna	Website,GitHub	RV64GC	Solderpad Hardware License v. 0.51
Riscy Processors	MIT CSAIL CSG	Website,GitHub		MIT
RiscyOO	MIT CSAIL CSG	GitHub	RV64IMAFD	MIT
Lizard	Cornell CSL BRG	GitHub	RV64IM	BSD

Name	Maintainer	Links	User spec	License
Minerva	LambdaConcept	GitHub	RV32I	BSD
OPenV/mriscv	OnChipUIS	GitHub	RV32I(?)	MIT
VexRiscv	SpinalHDL	GitHub	RV32I[M][C]	MIT
Roa Logic RV12	Roa Logic	GitHub	2.1	Non-Commercial License
SCR1	Syntacore	GitHub	2.2, RV32I/E[MC]	Solderpad Hardware License v. 0.51
Hummingbird E200	Bob Hu	GitHub	2.2, RV32IMAC	Apache 2.0
Shakti	IIT Madras	Website,GitLab	2.2, RV64IMAFDC	BSD
ReonV	Lucas Castro	GitHub		GPL v3
PicoRV32	Clifford Wolf	GitHub	RV32I/E[MC]	ISC
MR1	Tom Verbeure	GitHub	RV32I	Unlicense
SERV	Olof Kindgren	GitHub	RV32I	ISC
SweRV EH1	Western Digital Corporation	GitHub	RV32IMC	Apache 2.0
Reve-R	Gavin Stark	GitHub	RV32IMAC	Apache 2.0

What problem are we trying to solve?

Barriers to adoption of open-source cores

- IP quality
  - harness community best-in-class design and verification contributions
- Ecosystem
  - ensure availability of IDE, RTOS / OS ports, physical design etc. and create a roadmap of cores covering a range of PPA metrics
- Permissive use
  - permissive open-source licensing and processes to minimize business and legal risks

CORE-V™ Family of RISC-V Cores

- Initial contribution of open source RISC-V cores from ETH Zurich PULP Platform
  - Very popular, industry adopted cores
- OpenHW Group becomes official committer for these repositories

PULP
Parallel Ultra Low Power

CORE-V™

Core	Bits/Stages	Description
RI5CY	32bit / 4-stage	A 4-stage core that implements, the RV32-IMC, has an optional 32-bit FPU supporting the F extension and instruction set extensions for DSP operations, including hardware loops, SIMD extensions, bit manipulation and post-increment instructions.
Ariane	64bit / 6-stage	A 6-stage, single issue, in-order CPU implementing RV64IMCD extensions with three privilege levels M, S, U to fully support a Unix-like (Linux, BSD, etc.) operating system. It has configurable size, separate TLBs, a hardware PTW and branch-prediction (branch target buffer, branch history table and a return address stack).

Broad ecosystem enablement

1. Proven RTL core designs, processor sub-system IP blocks, verification test bench, and reference designs

2. Industry-proven IDEs, a wide range of RTOS/OS ports and extensive libraries to build necessary software stacks

3. Validated EDA tool flows and proven PPA characteristics

4. International footprint with developers in North America, Europe and Asia

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Why a new org?

- Why not part of the RISC-V Foundation, FOSSi Foundation, Free Silicon Foundation or CHIPS Alliance?

- Open-source, non-profit org with:
  - Freedom of action - a separate legal entity
  - Driven by major corporations and academia
  - Enable ‘SW to RTL to Physical’ of open-source cores and related IP for high volume production SoCs
  - Leverage proven industry CAD tools and EDA flows

OpenHW Group founding principles

- All OpenHW Group IP shall remain open source, license-free and available to all parties
- All OpenHW Group trademarks and certification marks are freely available to all parties for cores used in non-commercial offerings
- OpenHW Group membership is required to license trademarks and certification marks for cores used in commercial offerings
  - Marks, such as CORE-V, signify that cores have been validated including passing compliance tests

OpenHW Group purpose

- Official source for a specific roadmap of open-source processor cores
  - Maintain online source repositories and documentation
  - Promote adoption through online and live events
- Responsible for sustaining, evolving and open-source licensing of processor cores and hardware/software ecosystem
  - Responsive to changes in technology and needs of the user community
- Manage licensing of trademarks / certification marks decides whether a project or product can use the marks

OpenHW Group structure

- On behalf of the membership, Board of Directors responsible for fulfilling the organization's purpose
- Board appoints Chairs of working groups and has final approval of working group recommendations
  - Technical Working Group and Marketing Working Group will be standing working groups
- All working group participants must be organization members
- WG Chairs report to the Board
- WGs are subject to termination if not making satisfactory progress

Corporate Membership & Contributors

- Platinum Members – larger $ commitment + up to 3 Active Contributors
  - Platinum members are eligible for Board seat elections and to Chair Technical and Marketing Working Groups and sub Task Groups
- Gold Members – medium $ commitment + 2 Active Contributors
  - Gold members are eligible to Chair Technical and Marketing Working Groups and sub Task Groups
- Silver Members – smaller $ commitment
  - Silver members are eligible to participate in Technical and Marketing Working Groups and sub Task Groups
- Platinum, Gold and Silver members have one vote per member in all organizational or Working Group ballots / elections
- Associate Members (non-voting)
  - Associate members (non-profits, research labs & Universities) are eligible to participate in Technical and Marketing Working Groups and sub Task Groups without voting rights

Eclipse Foundation Partnership

- Well-defined, vendor-neutral, proven development process based on
  - Openness, Transparency, Meritocracy
- Predictable releases
- Industry-leading IP policy and due diligence
- All OpenHW Group corporate members will automatically be Eclipse Foundation members

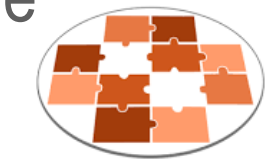
380+
Projects

195M+
Lines of Code

1550+
Committers

Individual contributors

- Individual contributors participate in OpenHW Group developments via a Contributor License Agreement (CLA)
- OpenHW Group has adopted the well-defined, vendor-neutral and proven Eclipse Development Process
  - Openness, transparency, meritocracy
- Individual contributor CLAs managed with user accounts on openhwgroup.org and the contributor's GitHub account
- The OpenHW Group is committed to work together with the FOSSi Foundation to reach out and support individual contributors



FOSSi Foundation

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Working Groups & Task Groups

- Board appoints Chairs of ad-hoc working groups and has final approval of working group recommendations
  - Technical Working Group and Marketing Working Group will be standing working groups
- Technical Working Group
  - Cores Task Group
  - Verification Task Group
  - Platform Task Group
- Marketing Working Group
  - Content Task Group
  - Events Task Group

CORES Task Group Charter

- Definition of the cores IP roadmap covering ISAs and micro-architectures for a variety of applications
  - Acceptance (via defined criteria), curation and subsequent development of donated core IP as initial constituents of the roadmap
  - Development and curation of new core IP as subsequent constituents of the roadmap
- Alignment and ratification of feature proposals and contributions from corporate members and the individual contributor community
- Planning and coordination of development efforts
  - Assignment of ownership and tracking specific core and feature developments
- Open-source delivery of production quality IP cores guaranteed to inter-operate with industry standard tools and flows (including relevant documentation)
- Generation and maintenance of CORE-V specific standards
  - Contribution to the RISC-V foundation via relevant proposals (as required)

Verification Task Group Charter

- Managing a collaborative, industry standard DV effort for the curated RTL cores, to ensure high quality RTL for use in high volume production SoCs
- Developing an open source System Verilog testbench including:
  - UVM generators, Directed Tests, and Compliance tests
- Setting quantitative DV targets and tracking DV progress for what is considered to be a high quality RTL core
- Accepting contributions from corporate members and the individual contributor community and curating that code to maintain an optimal set of tests

Platform Task Group Charter

- Define Hardware Platforms for our curated cores:
  - Embedded (bare metal / RTOS), Mid-range (Linux / FreeBSD), High-performance
  - Maximise alignment and help drive RISC-V Foundation platform efforts
- Define standard environments for supported cores & platforms:
  - Cores to be ubiquitous & interchangeable
  - Be specific about how to detect implementation details
  - Avoid the need for implementers to make platform-level decisions (avoid divergence + overhead)
- Write platform conformance tests:
  - Some tests specific to platforms (e.g. embedded, etc.)
  - Provide reference models for some components / reference implementations
- Facilitate platform software development:
  - Provide customised toolchain, IDE, OS, etc. that “just works” on platforms as defined.

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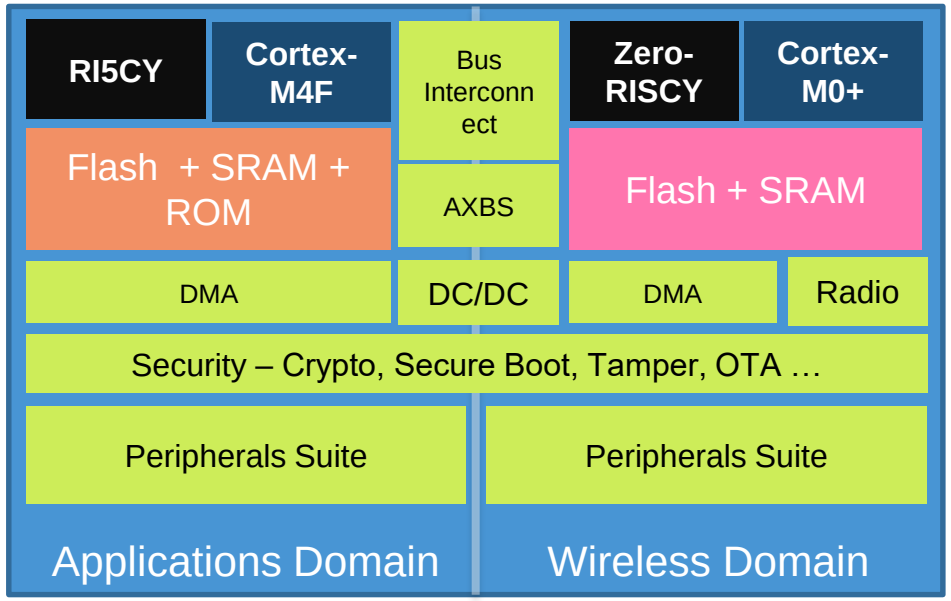
CORE-V NXP VEGA Demo

- Main application running on CORE-V (RI5CY) core
- BLE controller SW (Link Layer and PHY) running on Ibex (Zero-RISCY) core
- Micropython + drivers, all upstreamed and available on Github



VEGA

Zephyr™ Project

CORE-V Verification Test Bench Demo (proof of concept)

- Metrics: System Verilog simulator running on Google Cloud
- Imperas: Golden reference model of RISC-V CPU for comparison to DuT

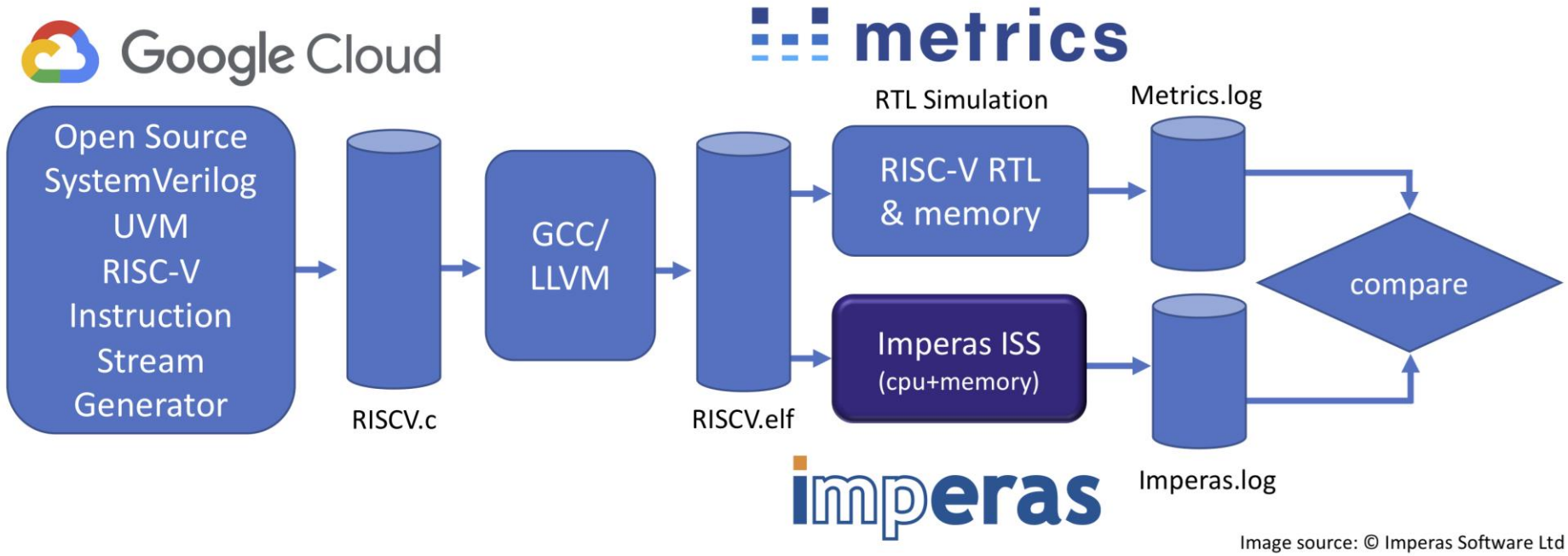
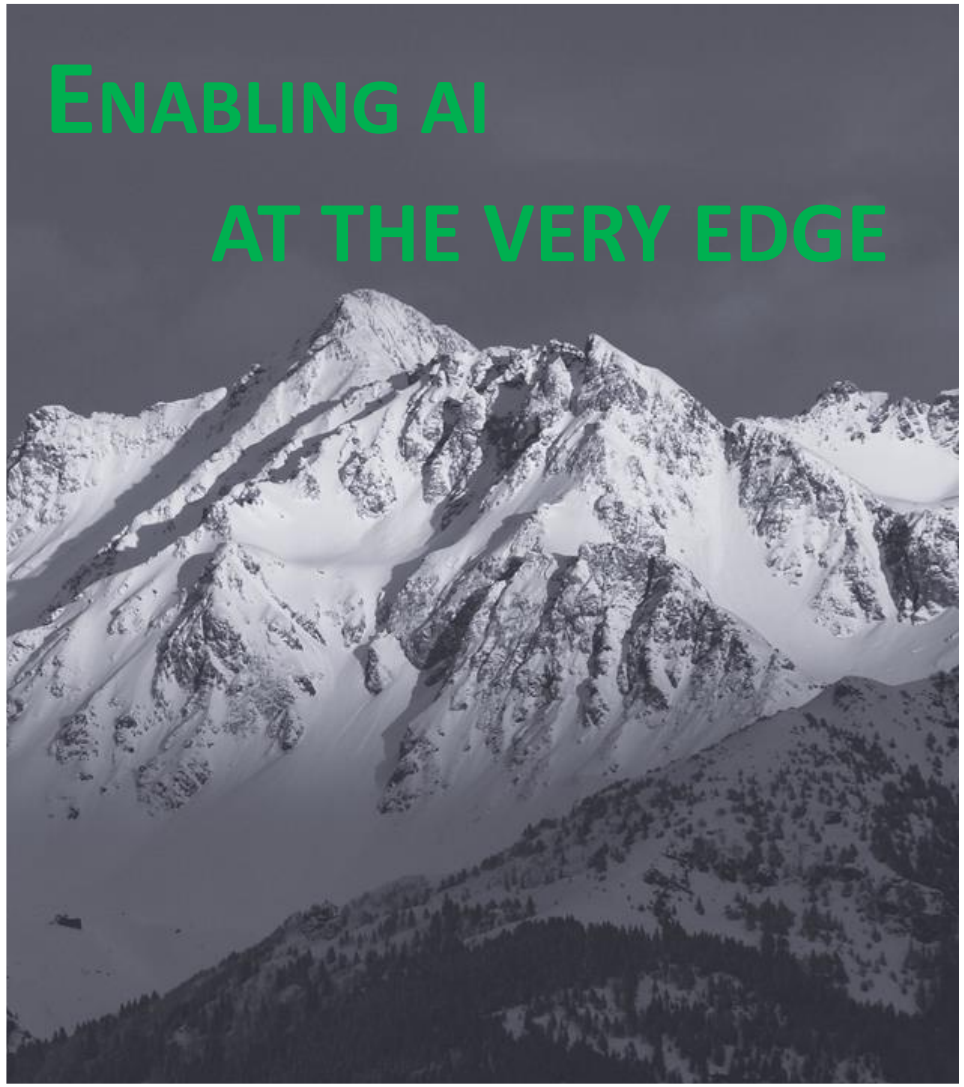


Image source: © Imperas Software Ltd

GreenWaves CORE-V Demo



GAP8

9 CORE-V RI5CY Cores

Interpret images, sounds and vibrations on battery operated sensors and devices

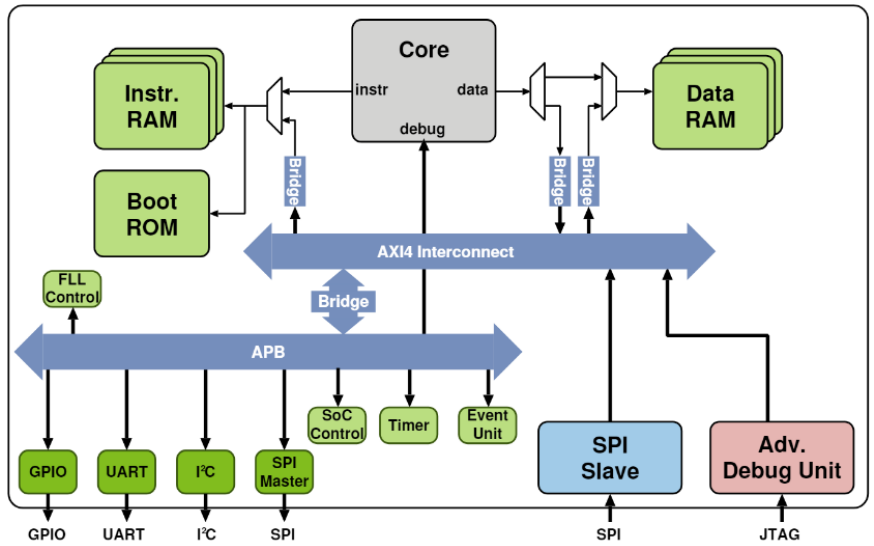
GREENWAVES TECHNOLOGIES

CORE-V™

OneSpin CORE-V Demo

OneSpin RISC-V Integrity Verification Solution

Demo: PULPino SoC with CORE-V **RI5CY** core



Learn more

Formal Verification of PULPino and other RISC-V SoCs

June 12, 13:35 – 13:50

Ask **nicolae.tusinschi@onespin.com** for a demo

Formal Apps

Automated checks (RI5CY, entire SoC)

Floating-point unit (FPU) verification

AXI4 and APB protocol compliance

I²C protocol compliance

…

RISC-V Verification App

Automate/Accelerate RISC-V Verification

Proof of correctness

Capture/verify custom extensions

Detect additional/undocumented logic

Unbounded proofs

Complete run in few hours

Summary

1. Strong support from industry, academia and individual contributors
2. Proven RTL core designs, processor sub-system IP blocks, verification test bench, and reference designs
3. Industry proven IDEs, a wide range of RTOS/OS ports and extensive libraries to build necessary software stacks
4. Validated EDA tool flows and proven PPA characteristics
5. International footprint with developers in North America, Europe and Asia