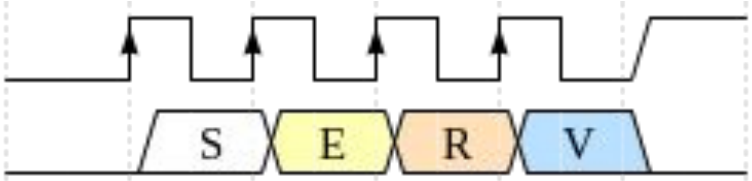


Bit by bit - How to fit 8 RISC-V cores in a $38 FPGA board

Olof Kindgren
Qamcom Research & Technology, FOSSi Foundation

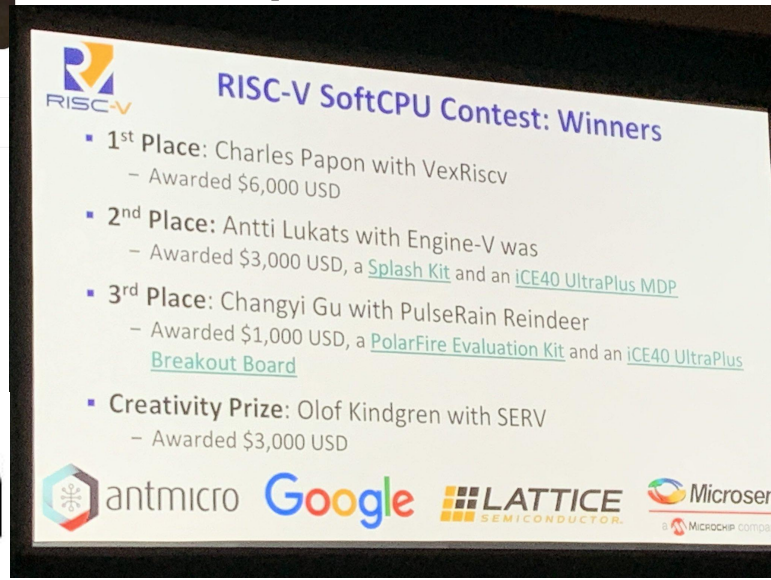
Who am I?

ORConf

Portland Oregon

LATCH-UP

May 4-5 2019

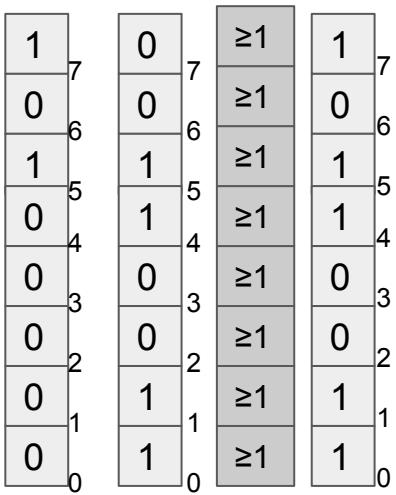


Award-winning

FOSSi Foundation

qamcom

What’s a bit-serial CPU?



A parallel CPU requires n or gates for an n-bit CPU

0xA0 | 0x33 = 0xb3

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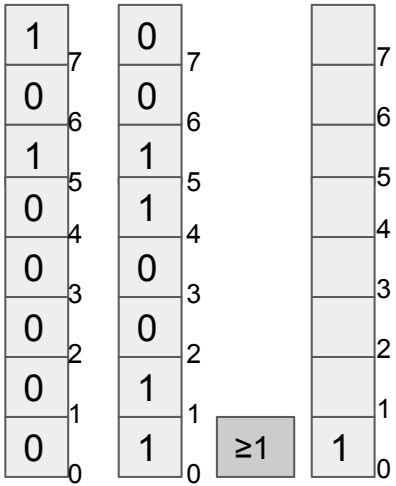

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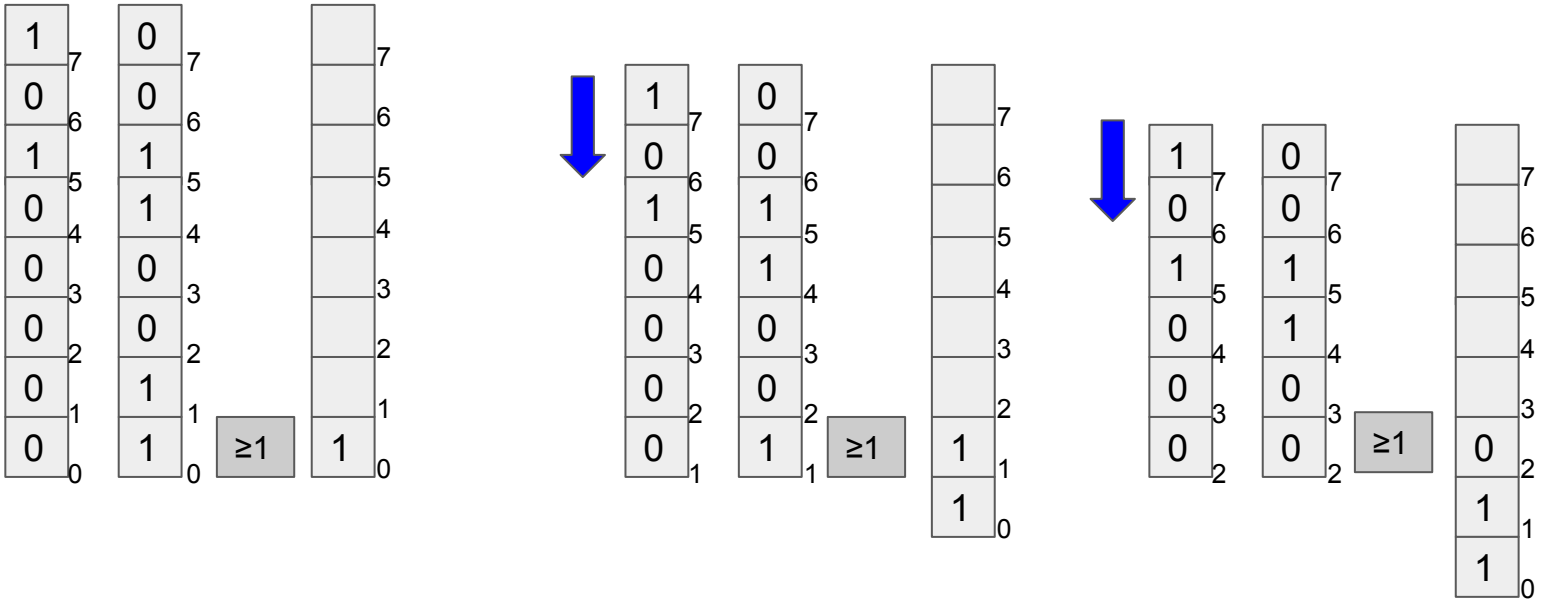

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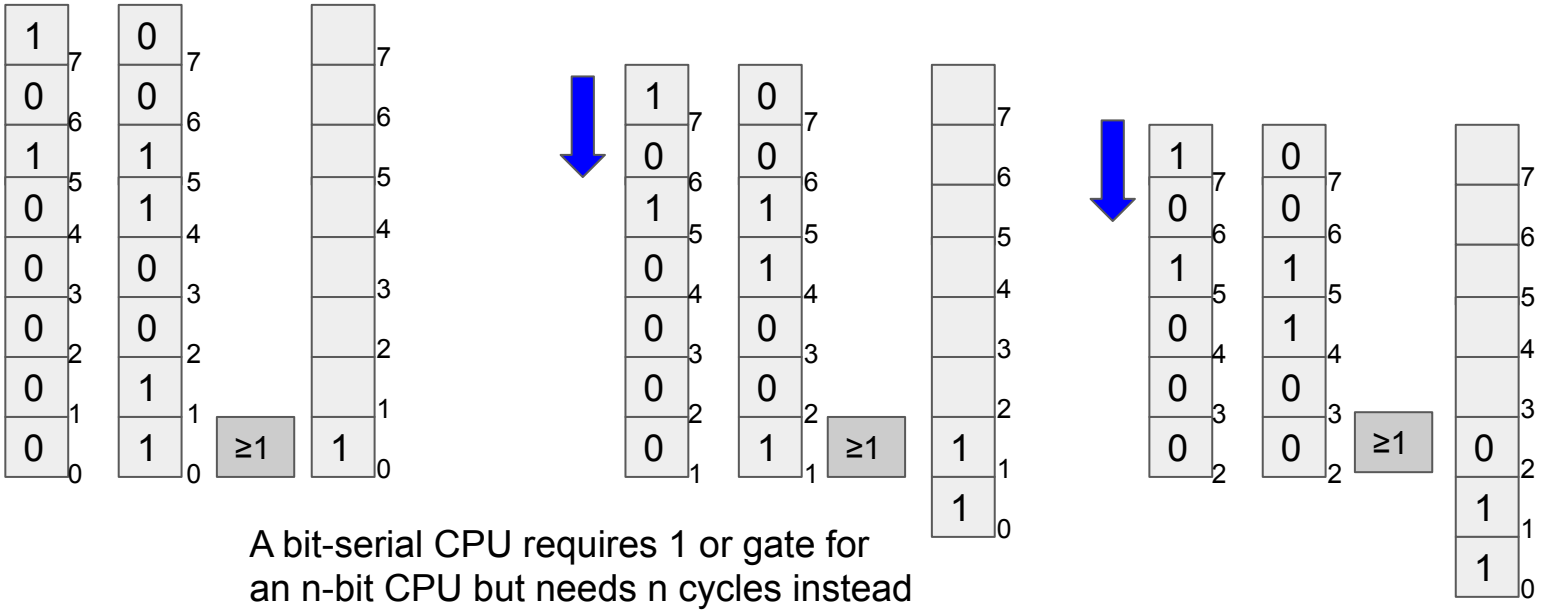
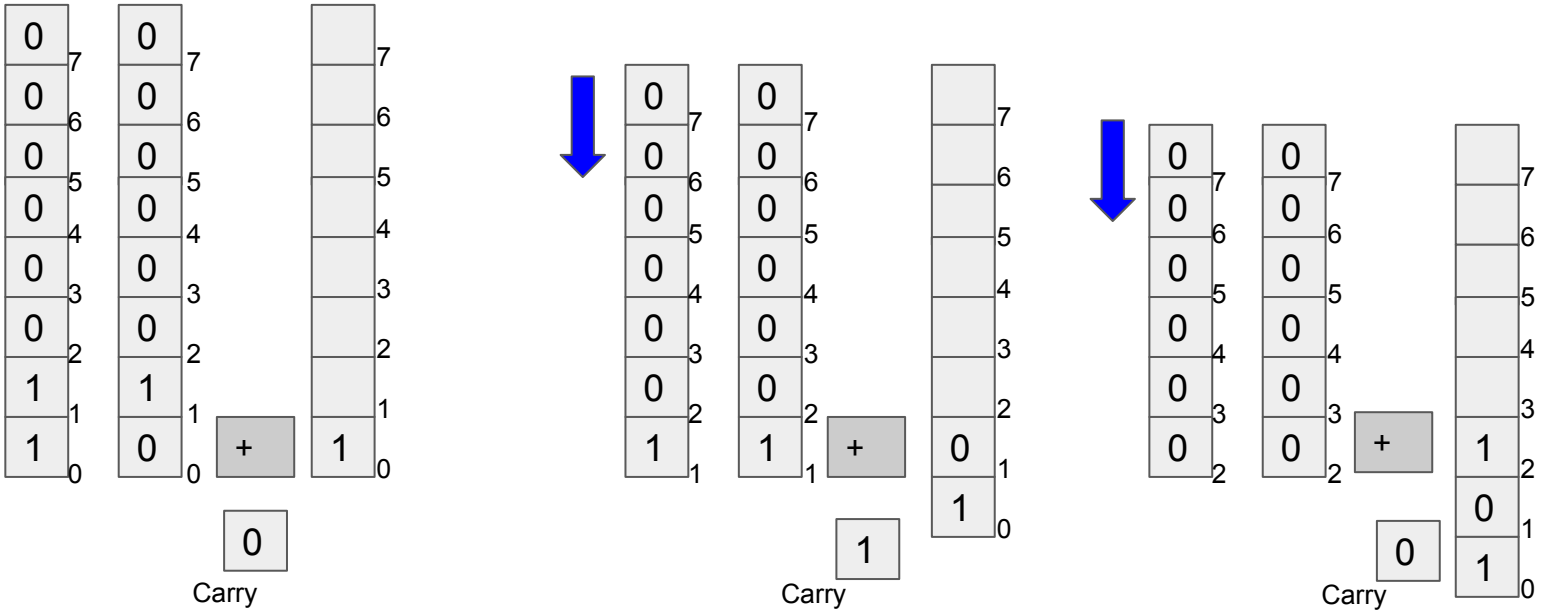


A bit-serial CPU requires 1 or gate for an n-bit CPU but needs n cycles instead

Trading speed for area

What's a bit-serial CPU?



0x03 + 0x02 = 0x05

Capabilities

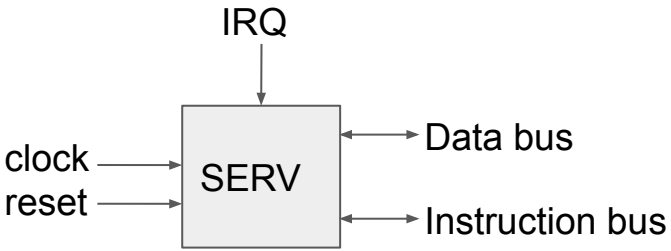
- RV32I with enough of privilege spec to run compliance tests and Zephyr
- Formally verified with RISCV-Formal
- Tested in hardware on TinyFPGA BX
- Packaged for FuseSoC
- BSD-licensed

Speed

- CPI
  - Most instructions take 32 cycles + memory fetch delay
  - Some instructions need 2x32 + memory fetch delay
    - Jumps => Need to calculate PC and check for exceptions before updating PC
    - Load/store => Need to check alignment before hitting the bus
    - SLT* => Instructions flow LSB->MSB but bit 0 needs to be set (Grr…!!!)
  - Shifts need 32 + a shift-amount dependent number of cycles
- Frequency
  - ~50MHz on iCE40
  - ~220MHz on Artix-7

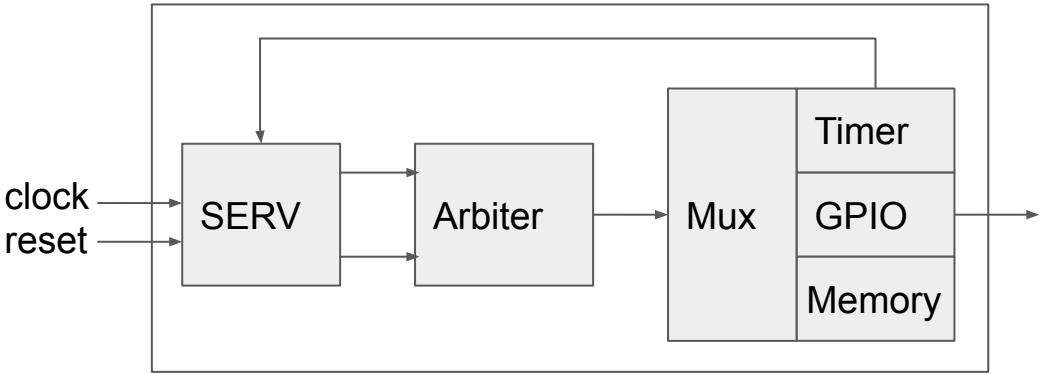
Naming conventions

SERV = CPU



Naming conventions

SERV = CPU
servant = Minimal SoC with SERV, timer, memory and GPIO. Enough to run Zephyr



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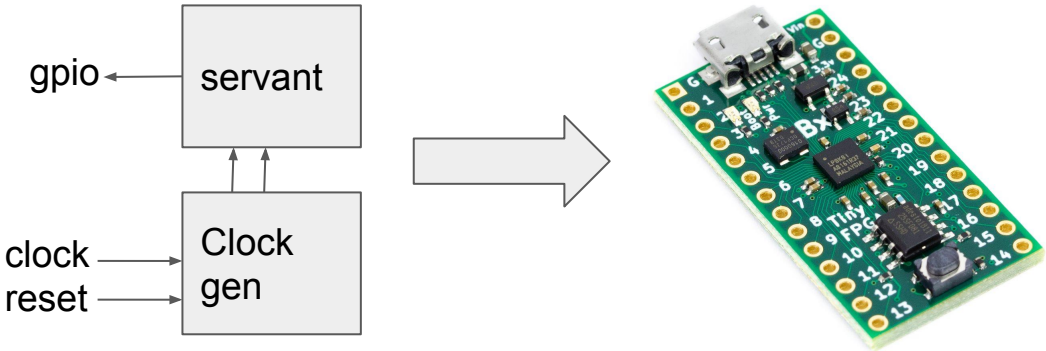

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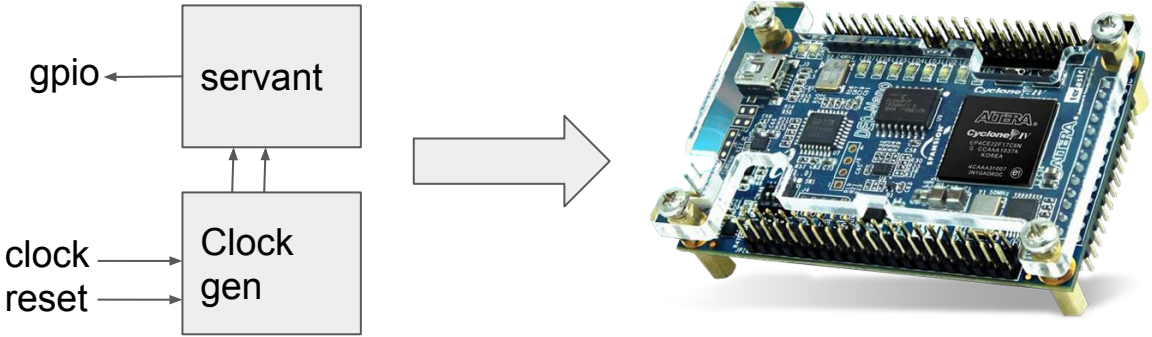

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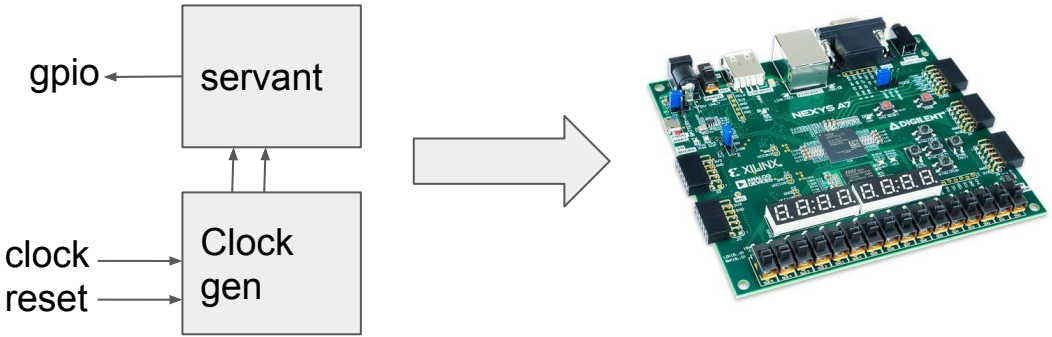

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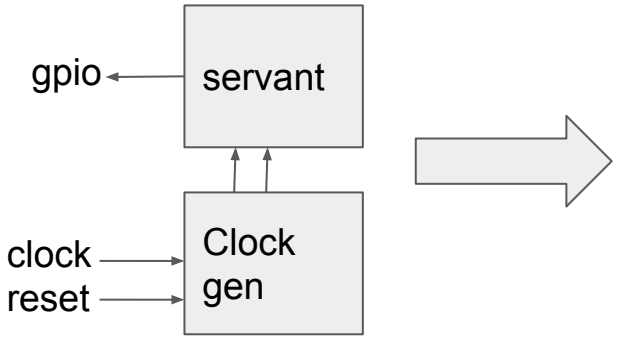
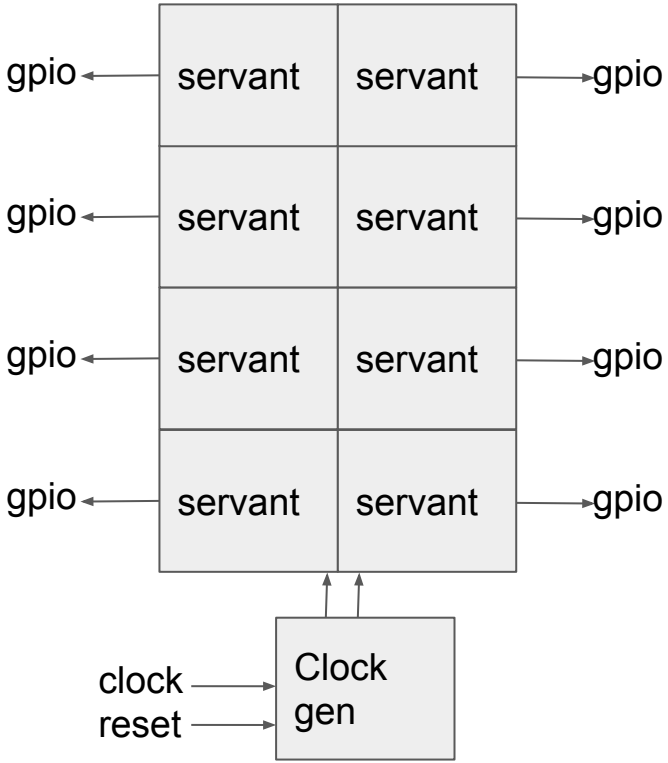
servix = servant implemented on Xilinx Artix
servESA = servant implemented in a chip that will be used by the European Space Agency



Naming conventions

serveral = A whole lotta servants



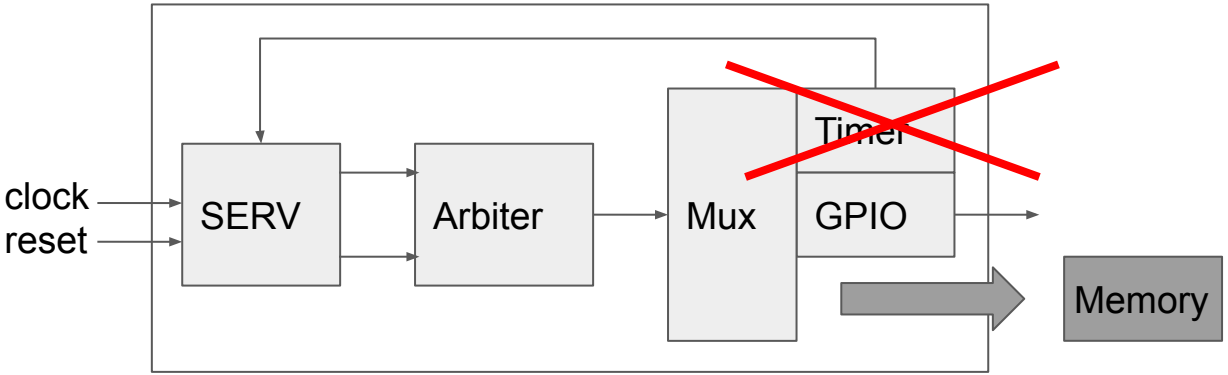
Size comparison

	TinyFPGA BX iCE40 hx8k	DE0 Nano Cyclone IV-E 22k	Digilent Nexys A7 Artix-7 100t
SERV (LUT/FF/RAM)	354/345/1	582/337/1	436/375/0
serveral (instances)	10 (out of memory)	33 (out of memory)	210 (out of memory)
$/servant	38/10=3.8	79/33=2.39	265/210=1.26

Can we do better?

More cores

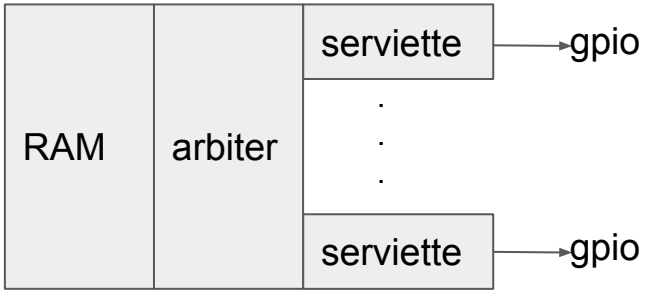
serviette = Minimal SoC with CSR-less SERV, memory port and GPIO. Enough to run bare-metal RV32i

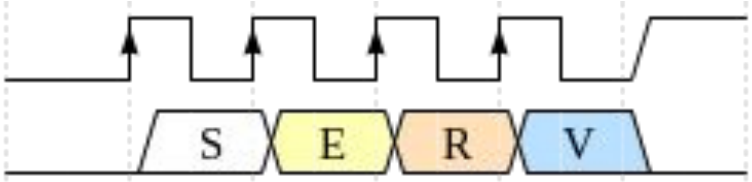


More cores

serviette = Minimal SoC with CSR-less SERV, shared memory and GPIO. Enough to run bare-metal RV32i

- serveral serviettes How many?
  - 16 to saturate memory
  - 2 seems to give best logic/memory balance





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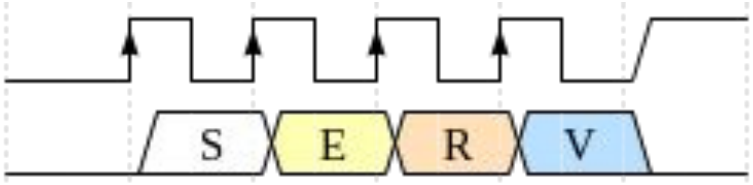
Use cases

- Power management
- Glorified FSM
- Control plane CPU
- Sensor hubs
- Embarrassingly parallel tasks

Future work

- Optimizations
  - Share code and register file to save a RAM
  - Global optimization of control signals from decoder
  - Fine-tune decoder for LUT size (optionally put it in RAM)
  - General LUT golfing
- Improvements
  - Implement C ISA extension
  - Run from SPI Flash
  - Add RX UART and hex bootloader



That's it folks!

https://github.com/olofk/serv

http://fusesoc.net

https://gitter.im/librecores/fusesoc

...unless you have questions

Don't miss...