PolarFire® SoC: A Secure, Low Latency, Heterogenous Compute Platform for the Edge

Ted Speers, Head of Product Architecture and Planning

RISC-V Zurich Workshop, June 11, 2019
Some Goals and Messages

- Why Microchip FPGA technology matters at the edge
- Historical perspective on Microchip FPGA BU’s involvement in RISC-V
- What PolarFire™ SoC can do for you
# Trends in Compute

## Megatrends

- **Exponential growth of connected devices and human machine interaction**

## Low Power

- 10 years on AAA battery
- POE (24W)

## Solution Trends

- Compute workloads and storage pushing out to devices and edge to reduce power and latency
- Hardware security solutions from device to gateway
- Need for safety and reliability increasing

## Gateways / Transport

- Gateways moving to the local premise to improve real-time speed
- Fan-less outdoor enclosures

## Data Center / Cloud

- Massive data being processed in the Cloud – creating latency
- Fixed power budget for 20-year lifetime of facility
- $6/W/yr
- Heterogeneous compute paradigms and accelerators
Megatrends

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“The” Edge

- The One and Only Edge Gateways / Transport
- Data Center / Cloud

- Compute workloads and storage pushing out to devices and edge to reduce power and latency

Microchip
Galaxy GN-z11, shown in the inset, is seen as it was 13.4 billion years in the past, just 400 million years after the big bang, when the universe was only 3 percent of its current age.

Image source: NASA
View of Pluto as *New Horizons* left the system, catching the Sun's rays passing through Pluto's atmosphere, forming a ring.

Image source: NASA
Edge of the Troposphere

~200,000 flights a day tracked by FlightRadar24
Common Denominator?
Microchip FPGAs at the EDGE

Boeing 787 Dreamliner

Pluto New Horizons
Pluto Images 2015

Hubble SM-4
WFC3 Install 2009

APA, A3P, AX

RTSX32SU, RTSX72SU

RH1280

Image sources: NASA
Number One From Low Earth Orbit to Beyond Pluto

**Rosetta**
Orbits and Lands on Comet 2014

**Pluto New Horizons**
Pluto Images 2015

**JUNO**
Entered Jupiter Orbit 2016

**IRNSS**
7 Satellites Launched 2013-2016

**GOES-R**
Climate Satellite Launched 2016

**Iridium Next**
First 10 Satellites Launched 2017

Image sources: NASA, ESA
Number One Above
30000 Feet

**Airbus A380**
- APA, A500K, SX-A, AX FPGAs
- Flight computers, cockpit displays, engine controls, power distribution...

**Boeing 787 Dreamliner**
- APA, A3P, AX FPGAs
- Flight computers, cockpit displays, engine controls, braking, power distribution, cabin pressure, flight surface actuation...

**Boeing 777-300ER**
- A3P, Igloo2 FPGAs
- Flight computers, power distribution, engine controls, electronic control networks, flight surface actuation...

**Airbus A350 XWB**
- APA, A3P FPGAs
- Flight computers, cockpit displays, braking, engine controls, power distribution, cabin pressure, flight surface actuation...
Electronic devices experience neutron effects up to 500 times more frequently at aviation altitudes than at sea level.
Securing the Edge From Womb to Tomb

FIPS 140-2 Level 3
Hardware Security Modules (HSMs)

Authenticate ICs w/ Silicon Secrets

Factory Keys

ECC Key Pairs

Fabrication
- Secrets “baked” into Silicon

Wafer Test
- Authenticate ICs using Silicon Secrets
- ICs Authenticate Microsemi HSMs, too
- Inject Symmetric Factory Keys & S/Is
- Inject ECC Key Pairs & Enroll ECC Private Keys with Physically Unclonable Functions (PUFs)
Low PolarFire® Power Enables the Edge

Edge of Pain

>8 Watts (Competitor)

8 Watts (PolarFire)
Trends in Compute

Megatrends
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Where Microchip FPGAs Play

Megatrends

Low Power

Solution Trends

Device / Sensors / Actuators

Exponential growth of connected devices and human machine interaction

Gateways / Transport

Gateways moving to the local premise to improve real-time speed

Fan-less outdoor enclosures

Data Center / Cloud

Massive data being processed in the Cloud – creating latency

• Fixed power budget for 20-year lifetime of facility
  • $6/W/yr

Compute workloads and storage pushing out to devices and edge to reduce power and latency

Hardware security solutions from device to gateway

Need for safety and reliability increasing

Heterogeneous compute paradigms and accelerators

• 10 years on AAA battery
  • POE (24W)
Shifting From Red to Blue

- **March 2010 – Shipped SmartFusion®**
  - Industry’s first ‘SoC FPGA’
  - Microcontroller based
- **October 2012 – Announced SmartFusion® 2**
Shifting From Red to Blue

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  - Microcontroller based
- October 2012 – Announced SmartFusion® 2
Unseen Force

Linux v Real-time Market

Data Source: Extrapolated from VDC Research 2015
December 8 - 12, 2014

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Shifting From Red to Blue

- **March 2009** – Announced SmartFusion®
  - Industry’s first ‘SoC FPGA’
  - Microcontroller based
- **October 2012** – Announced SmartFusion® 2
- **December 9, 2014** – Microchip FPGA BU discovers RISC-V
Real-Time Linux?

- **Wide spread Linux adoption**
  - Rich OS with thousands of applications to choose from

- **Requirements still exist for real-time while running Linux**
  - Safety critical
    - The ability to deterministically monitor the execution environment.
  - Real-time system control
    - Completing tasks deterministically, on time every time.
  - Securing the IoT
    - Execute a trusted execution environment deterministically for consistent results.

- **Working with our partner** SiFive
  - We have been able to architect a complex SoC FPGA that provides
    - Determinism and a rich OS within the same multi-core CPU cluster
Introducing PolarFire® SoC

Freedom to innovate in:
• Linux® and real-time
• Thermal and power constrained systems
• Securely connected IoT systems
• High-rel safety critical systems

HARDENED RISC-V SUBSYSTEM
PolarFire® SoC RISC-V-Based SoC FPGA

Freedom to innovate in:
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Measured ISR Execution Time in Quad Core CPU

- Periodic Interrupts
  - $T_0 = T_1$
- Inconsistent Execution Times
  - $E_0 \neq E_1 \neq E_2$
Flexible Memory Sub-System Provides ISR Determinism

- Periodic Interrupts
  - $T_0 = T_1$
- Consistent Execution Times
  - $E_0 = E_1 = E_2$

Disable branch predictor during critical code execution, or permanently.
Coherent Message Passing in AMP Systems

- L2 Cache for SMP Cluster
- L2 LIM for Real-Time
- L2 Scratchpad for Coherent Message Passing
PolarFire® SoC
RISC-V-Based SoC FPGA

Freedom to innovate in:
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Secure Boot

- Guards against sophisticated methods of attack whereby a malicious external agent tampers with the boot image stored in bootflash (e.g. Linux FSBL).
- Authenticates the image in bootflash before transferring execution control to the OS boot loader pointed to by reset vector.
- FPGA system controller (root of trust) manages the authentication process and certifies boot image using crypto functionality built into the FPGA backbone.
  - Push “zero state boot loader” (ZSBL) upon detecting HW reset.
  - Releases monitor core from reset and executes authentication on FSBL image pointed to by reset vector.
  - If authentication is successful, transfer execution control back to FSBL, otherwise abort.
Our solution caters to low power, high-speed, secure, real-time applications.

- **Machine Vision**
  - Secure communication
  - High speed I/O

- **Surveillance Systems**
  - 4k resolution
  - Image sensor muxing

- **Drone Cameras**
  - Low power
  - Hi-reliability
  - IP security

- **Medical Imaging**
  - Security
  - High speed I/O
  - Instant on

- **Machine Learning**
  - Hi-reliability
  - High speed I/O
  - 4K resolution

PolarFire® has robust DSP and Memory resources that are key criteria in Smart Embedded Vision applications.
Freedom to Begin Hardware Development

PolarFire SoC Embedded Experts Development Platform
Freedom to Start Software Development

- Free rapid software development and debug capabilities without hardware
- Complete PolarFire SoC processor
- Subsystem model
Mi-V™ RISC-V Ecosystem

- A continually expanding, comprehensive suite of tools and design resources to fully support RISC-V designs.

- Aims to increase adoption of RISC-V ISA and Microchip's soft CPU product family.

- Supports development using Microchip’s soft-CPUs and RISC-V SoC FPGAs
Recipe For the New Golden Age

- Open Instruction Sets
- Enhanced Security
- Agile Chip Development
- Domain Specific HW/SW Co-Design

stay tuned
Thank You