PULP Platform, what’s next?

Six years of working on open source hardware

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PULP started in 2013

- Luca wanted to work on **NEW** energy efficient architectures
  - Keywords were: parallel processing, near threshold operation, energy efficiency
  - **P**arallel **U**ltra **L**ow-**P**ower platform was born

- Large group of **60 people** in ETH Zurich and University of Bologna
  - Working on technology, IC design, architecture, programming, and applications.

- By the end of this month, we will have **34 ASICs** taped out
  - **4x** 22nm, **4x** 28nm, **1x** 40nm, **15x** 65nm, **5x** 130nm, **5x** 180nm

  + 5 more that still need pictures
Committed to open source from day one

- Our goal was to release everything (we could) as open source
  - There are still discussions on what can be released (HDL source, scripts, netlist, GDS)
  - PULP has been using a permissive Solderpad license since the beginning

- Our first open source release was in February 2016 (PULPino)
  - Very simple microcontroller using a single 32-bit RISC-V core (RI5CY)

- As of now (2019) we have released:
  - Single core platforms: PULPino, PULPissimo
  - Cluster-based multi-core platforms: OpenPULP, HERO, Open Piton + Ariane
  - And a range of RISC-V cores, peripherals, accelerators and interconnect solutions
Open source hardware is a necessity for us

- Allows us to collaborate more easily with partners
  - Both with academia and industry. Agreements are simpler (Back/Foreground is open source)
  - Can work with more people, can start faster, we can reuse what we develop in one project

- Leverage the community
  - Even a large academic group can not manage to support everything.

- Fair benchmarking
  - Everyone can verify our performance claims. Ultimately this will improve quality of results

- Open source solutions may help issues with Security and Safety
  - There is a lot of research interest in these domains.
- TSMC 40LP
  - Multi-cluster IoT processor
  - Similar to GAP8 of Greenwaves

- w/ Dolphin Integration
  - Power management IP

- Win-win for both
  - We get to use State of Art IP
  - Dolphin can show their IP working in a complete system.
Arnold - 2019

- GF 22 FDX
  - Demonstrator (not a product)

- Cooperation w/Quicklogic
  - PULPissimo system paired with
  - Aurora eFPGA

- In 1 year from idea to chip
  - Fast collaboration
  - Wouldn’t have been possible without open source hardware
Kosmodrom - 2019

- GF22 FDX
  - Test chip with 2x Ariane (RV64)
- With Globalfoundries
  - Design methodology for energy efficient design
  - Body basing solutions (together with Invecas)
- Demo vehicle
  - We get access to new technology
  - GF gets a portable benchmark
You can buy development boards with PULP
As a university our goal is research

- We develop new architectures
  - We rely on open source cores
  - But core development is not our business
- Technical support needed
  - Documentation
  - User support
  - Design-for-Test solutions for production
  - Production level verification
- Not easy in an academic env.
Micro/Zero riscy is now Ibex

- **LowRISC** has agreed to maintain micro/zero riscy
  - Interested in using the core in their projects
  - They have a team that can provide support
  - ETH Zürich and University of Bologna will continue to contribute to Ibex

- **Our core has grown and left the house**
  - Alpine Ibex (*Capra Ibex*) is a mountain goat that is typical in the mountains of Switzerland
OpenHW Group launches CORE-V

- OpenHW group was founded by Rick O’Connor to:
  
  “boost the adoption of open-source processors by providing a platform for collaboration, creating a focal point for ecosystem development, and offering open-source IP for processor cores.”

- ETH Zürich is a founding member of OpenHW Group
  - The RI5CY and Ariane cores will continue to be maintained as part of Core-V
  - ETH Zürich and University of Bologna will continue to contribute to these cores
  - But now we will also have additional technical support from experts as well.
We are excited about the future of PULP

- Our cores have found homes that will take excellent care of them
  - Micro/Zero-riscy is being maintained by LowRISC as Ibex
  - RI5CY and Ariane will be maintained as part of Core-V project of OpenHW Group

- This support will result in better cores

- And it will allow us to concentrate on what we do best:
  - Developing new and efficient architectures using the building blocks we have
  - We already have several ideas that we are working on,
  - Stay tuned...
Any Questions??