<table>
<thead>
<tr>
<th>BM Series</th>
<th>BI Series</th>
<th>BR Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>BM-310 RV32IMC</td>
<td>BI-350 RV32IMAC[F]</td>
<td>BR-x51 (planned 2019)</td>
</tr>
<tr>
<td>BI-651 RV64GC</td>
<td>BI-671 RV64GC</td>
<td></td>
</tr>
</tbody>
</table>

- **BM Series**
  - Microcontroller core
  - Small and efficient
  - Low latency interrupts
  - Configurable for use case
  - IoT SoC
  - Sensor Fusion
  - Smart Meters
  - Accelerator control
  - Wearables

- **BI Series**
  - Linux capable application cores
  - From tiny to high-end cores
  - Single, Dual-issue and out-of-order designs
  - Multi-core support
  - Advanced IoT nodes, gateways
  - Artificial intelligence
  - Industrial automation
  - Storage applications
  - Networking applications
  - Datacenter applications

- **BR Series**
  - Embedded cores
  - Latency sensitive apps
  - High throughput
  - Real-time capabilities
  - Workload optimized
  - High performance ctrl
  - Baseband control
  - Modem L2/L3 processing
  - Low latency networking
  - SSD controllers
  - Compute/Accelerator
Custom SoC platforms

- Low Power MCU / Sensor Hub
  - BM Series based
- Motor control / Predictive maintenance
  - BR Series based
- Application processor / AI edge processor
  - BI Series based
Partner introduction

Milandr

- 130 IC design engineers
- Full cycle ASIC design
  - Analog RF design
  - Power management
  - Backend design
  - Digital design
  - IP design
  - Package design

- 150+ completed ASICs
- Experience with 22nm-180nm
- MCUs, Ethernet, Transceivers, ADC/DAC, RF
- New SoCs based on RISC-V!

- Assembly and test house
- 50 engineers
Custom SoC turnkey design service

CloudBEAR

Processor IP
Infrastructure IP

Customer requirements
Customer IP

Milandr
+own IP

Third party IP

Mass production chip
Low power MCU / Sensor hub platform

- BM series coreplex
- On-chip Flash
- Power management
- Voltage Controller
- Internal RC oscillators
- 12-bit SAR ADC
- UART
- SPI
- I2C
- 24-bit ΣΔADC
- PWM Timers
- RTC
- WDGs
- Your Custom IP

- TSMC 180nm
- TSMC 90nm LP
- RISC-V
- Integrated Flash for BOM cost reduction
- Main and battery power domains
- Voltage/Freq control
- ADCs with different precision and speed
- Temp sensor
**BM-310**

Microcontroller core

- Small, Low power microcontroller
- RV32IMC
- Machine/User privilege levels
- 3-stage pipeline
- Configurable interrupt controller

### Performance using GCC (per MHz)

<table>
<thead>
<tr>
<th></th>
<th>CloudBEAR BM-310</th>
<th>SiFive E21</th>
<th>ARM Cortex-M4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coremark</td>
<td>1.38</td>
<td>1.25</td>
<td>1.6</td>
</tr>
<tr>
<td>Dhrystone</td>
<td>2.76</td>
<td>2.5</td>
<td>1.38</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>TSMC 40LP, 9t</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency @ worst</td>
<td>200 MHz</td>
</tr>
<tr>
<td>Complex area (w/o TCM)</td>
<td>0.05 mm^2</td>
</tr>
<tr>
<td>Worst setup corner</td>
<td>SS, -40C, 0.81V</td>
</tr>
</tbody>
</table>
Motor control / Predictive maintenance platform

- TSMC 90nm LP
- Motor control
- Predictive Maintenance
- Automotive
- Lock-step, fault-tolerant

BR series coreplex

Isolated security/crypto subsystem

- BM-310
- Key RAM
- TRNG
- Crypto Acc

On-chip Flash
- 1 MiB

12-bit
- 3xADC
- 32 channels

12-bit
- 3xDAC

Your Custom IP

Motor Control Acc

UART, SPI, CAN, I2C

Ethernet

USB 2.0 PHY

PMU
- 3xLDO + DC-DC

Battery domain

High Freq PWM

169x193
Motor
Control
Acc

High Freq
PWM

USB 2.0 PHY

On-chip Flash
- 1 MiB

12-bit
- 3xADC
- 32 channels

12-bit
- 3xDAC

Your Custom IP
Application processor platform

- TSMC 28nm
- TSMC 40nm
- Pre-integrated platform with RISC-V application cores
- All SoC infrastructure included
- Targets
  - AI edge devices
  - Gateways
  - Industrial automation
BI series
Linux capable application cores

**BI-350**
RV32IMAC[F]

- 32-bit Tiny Linux capable core targeting IoT applications

**BI-651**
RV64GC

- 64-bit Linux capable core targeting high performance in power constrained environment

**BI-671**
RV64GC

- 64-bit Mid-range application core for maximum single thread performance
BI series core complex
Linux capable application cores

- RV64GC
- Multi-core fully coherent configuration
- Machine/User/Supervisor modes
- 32 KiB 8-way I/D caches
- L2 cache 1-2 MiB
- Debug module
- Platform Level Interrupt Controller
- Coherency controller for maintaining coherency with peripherals and accelerators
BI-671 mid-range OoO application core

- Mid-range performance
  - 2x comparing single-issue, 1.5x dual-issue designs
- Maximize power efficiency for given performance

1. Next PC
2. I$ access
3. I$ hit/miss
4. Branch Decode
5. BTB/BHT
6. RAS
7. RAS push
8. Issue Q
9. Issue Q
10. Issue Q
11. Issue Q
12. Issue Q

- Decode
- Rename
- RF access

- ALU0
- MUL
- ALU1
- DIV iter
- Branch
- LSU
- D$ access

- WB
BI-671 at a glance

- 10 stage pipeline
- Fetch 8B per cycle
- Decode two instruction per cycle
- Reorder buffer 48 entries
- Load/Store queues 16 entries each
- 4R3W integer register file 64 entries
- I-TLB, D-TLB 16 entries each
- Hardware page walk 4 entries
- 4-way BTB 512 entries
- 8-way 32KiB L1 I- and D-caches
- Out-of-order issue
  - 2 ALUs, 1 Branch, 1 Load/Store, 1 FP

<table>
<thead>
<tr>
<th></th>
<th>TSMC 28HPC+, 12t</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency @ worst SSG</td>
<td>1.2+ GHz</td>
</tr>
<tr>
<td>Dual core + L2 1 MiB</td>
<td>4.5-5 mm^2 *</td>
</tr>
</tbody>
</table>

* including all necessary SRAMs
**BI-671 at a glance**

- 1.3-1.4x better performance than ARM A9 and BOOMv2
- On the same performance level with MIPS P5600
- 75-80% of ARM A73, ARM A57, ET Maxion performance

<table>
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<th>Benchmark</th>
<th>Score/MHz</th>
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<tbody>
<tr>
<td>Dhrystone</td>
<td>3.58</td>
</tr>
<tr>
<td>Coremark</td>
<td>5.36</td>
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</table>
BI-671 SPEC2006 performance

BI-671 data is preliminary and collected on FPGA prototype.
bzip2, gcc, mcf – missing data for Zynq-7000 since require 2GiB RAM
gobmk, hmer, libquantum, astar – missing data for BOOMv2
BI-651 power efficient application core

- Power efficient dual issue core
- High performance in power constrained Linux-capable devices
## BI-651 performance

<table>
<thead>
<tr>
<th>Dhrystone performance comparison</th>
<th>BI-651</th>
<th>SweRV Late ALUs* off</th>
<th>SweRV Late ALUs on</th>
</tr>
</thead>
<tbody>
<tr>
<td>BTB=512 BHT=2048 RAS=8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GCC 8.2</td>
<td>2.44</td>
<td>2.10</td>
<td>2.36</td>
</tr>
<tr>
<td>Coremark performance comparison</td>
<td>BI-651</td>
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<tr>
<td>GCC 8.2</td>
<td>3.96</td>
<td>3.84</td>
<td>4.68</td>
</tr>
<tr>
<td>GCC 7.2</td>
<td>4.12</td>
<td>4.14</td>
<td>4.87</td>
</tr>
</tbody>
</table>

* Late ALU option was disabled for apple-to-apple comparison with SweRV core BI-651 Late ALU option under implementation.
Cycle-accurate simulation shows similar to SweRV Coremark performance.
BI-651 data is preliminary and collected on FPGA prototype.
BI-350 small Linux capable core

- Architecture: RV32IMAC[F]
- Single instruction issue
- Machine, Supervisor and User modes
- Configurable caches
  - Smaller size
  - Shorter cache line
  - Narrow memory interfaces
- L2 optional
- Tiny coherency controller configuration
- Configurable BTB, BHT, RAS

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www.cloudbear.ru