CloudBEAR

Processor IP product line

Products

Configurable and extensible 32/64-bit RISC-V cores

CloudBEAR

BM Series

BM-310

RV32IMC

- Microcontroller core
- Small and efficient
- Low latency interrupts
- Configurable for use case

IoT SoC
Sensor Fusion
Smart Meters
Accelerator control
Wearables

BI Series

BI-350

RV32IMAC[F]

BI-651

RV64GC

BI-671

RV64GC

- Linux capable application cores
- From tiny to high-end cores
- Single, Dual-issue and out-of-order designs
- Multi-core support

Advanced IoT nodes, gateways
Artificial intelligence
Industrial automation
Storage applications
Networking applications
Datacenter applications

BR Series

BR-x51 BR-x71

(planned 2019)

- Embedded cores
- Latency sensitive apps
- High throughput
- Real-time capabilities
- Workload optimized

High performance ctrl
Baseband control
Modem L2/L3 processing
Low latency networking
SSD controllers
Compute/Accelerator

Custom SoC platforms

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Low Power MCU / Sensor Hub	Motor control / Predictive maintenance	Application processor / AI edge processor
BM Series based	BR Series based	BI Series based

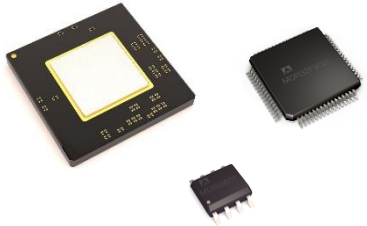
Milandr

Partner introduction

CloudBEAR

Milandr

- 130 IC design engineers
- Full cycle ASIC design
  - Analog RF design
  - Power management
  - Backend design
  - Digital design
  - IP design
  - Package design

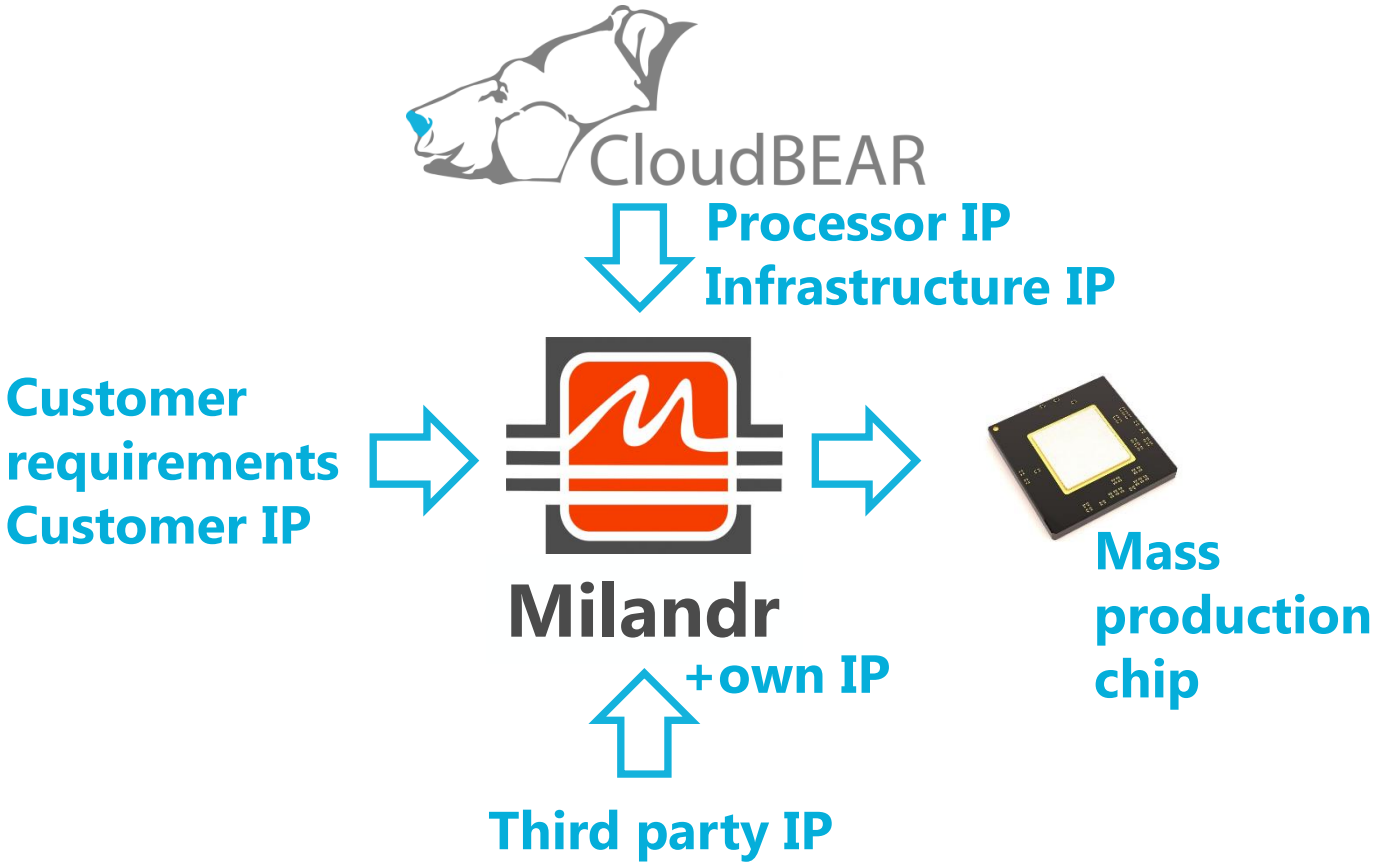


- 150+ completed ASICs
- Experience with 22nm-180nm
- MCUs, Ethernet, Transceivers, ADC/DAC, RF
- New SoCs based on RISC-V!

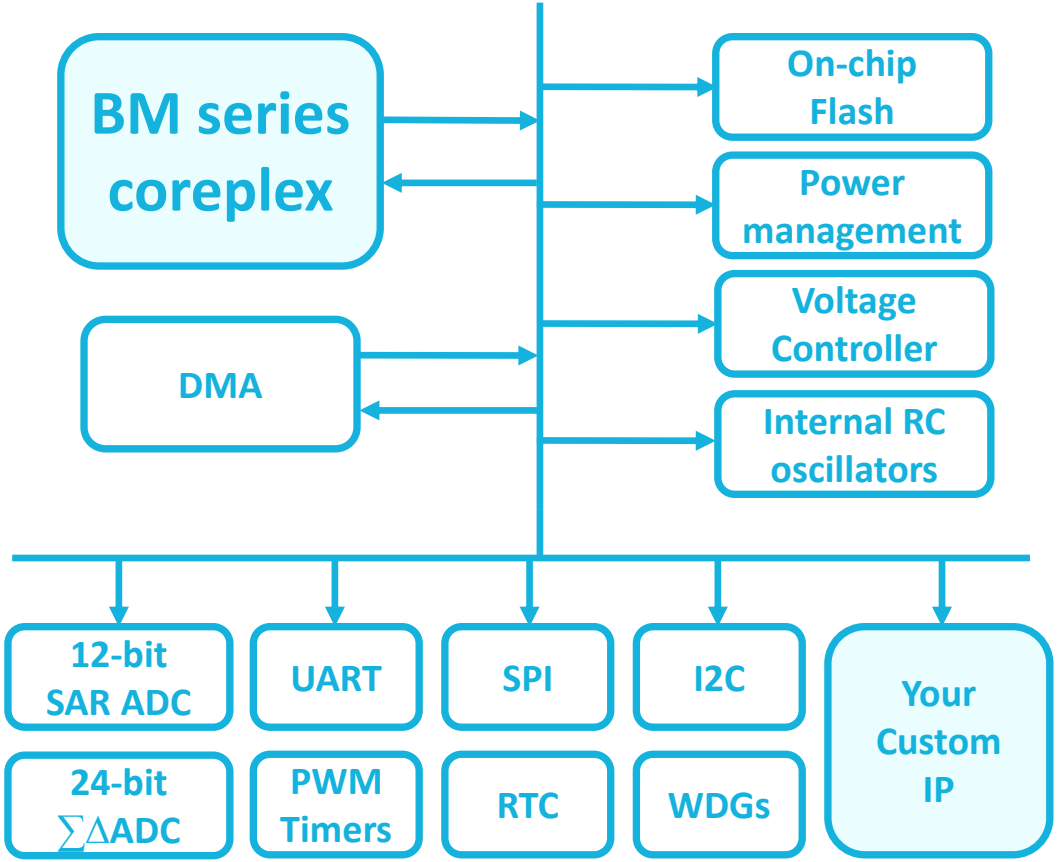
tsmc GLOBAL FOUNDRIES FAB TOWERJAZZ MIXED-SIGNAL FOUNDRY EXPERTS HHGrace

- Assembly and test house
- 50 engineers

Custom SoC turnkey design service



Low power MCU / Sensor hub platform



- TSMC 180nm
- TSMC 90nm LP

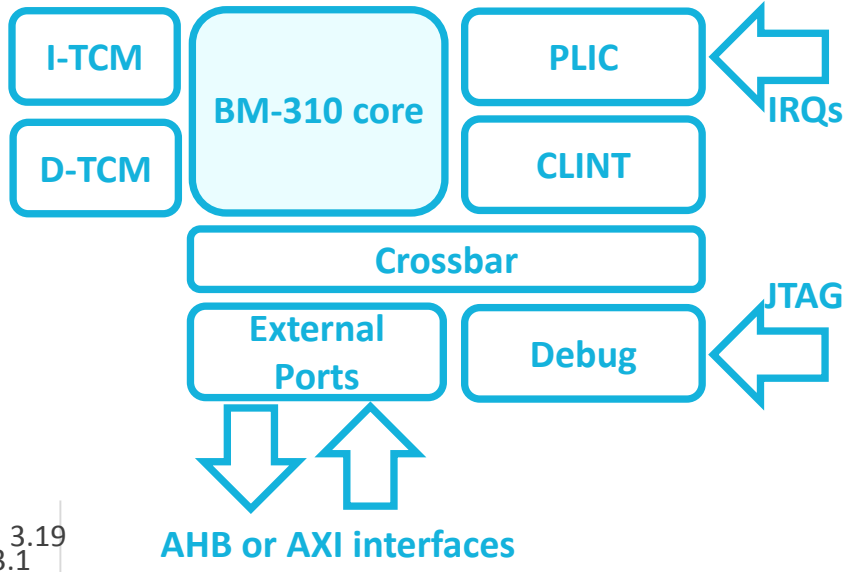
Milandr

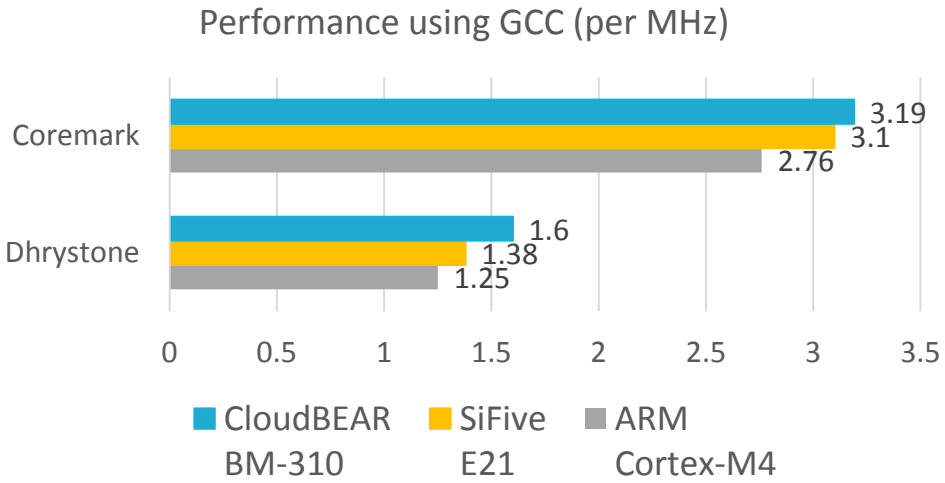
- RISC-V
- Integrated Flash for BOM cost reduction
- Main and battery power domains
- Voltage/Freq control
- ADCs with different precision and speed
- Temp sensor

BM-310

Microcontroller core

- Small, Low power microcontroller
- RV32IMC
- Machine/User privilege levels
- 3-stage pipeline
- Configurable interrupt controller





	TSMC 40LP, 9t
Frequency @ worst	200 MHz
Complex area (w/o TCM)	0.05 mm^2
Worst setup corner	SS, -40C, 0.81V

Motor control / Predictive maintenance platform

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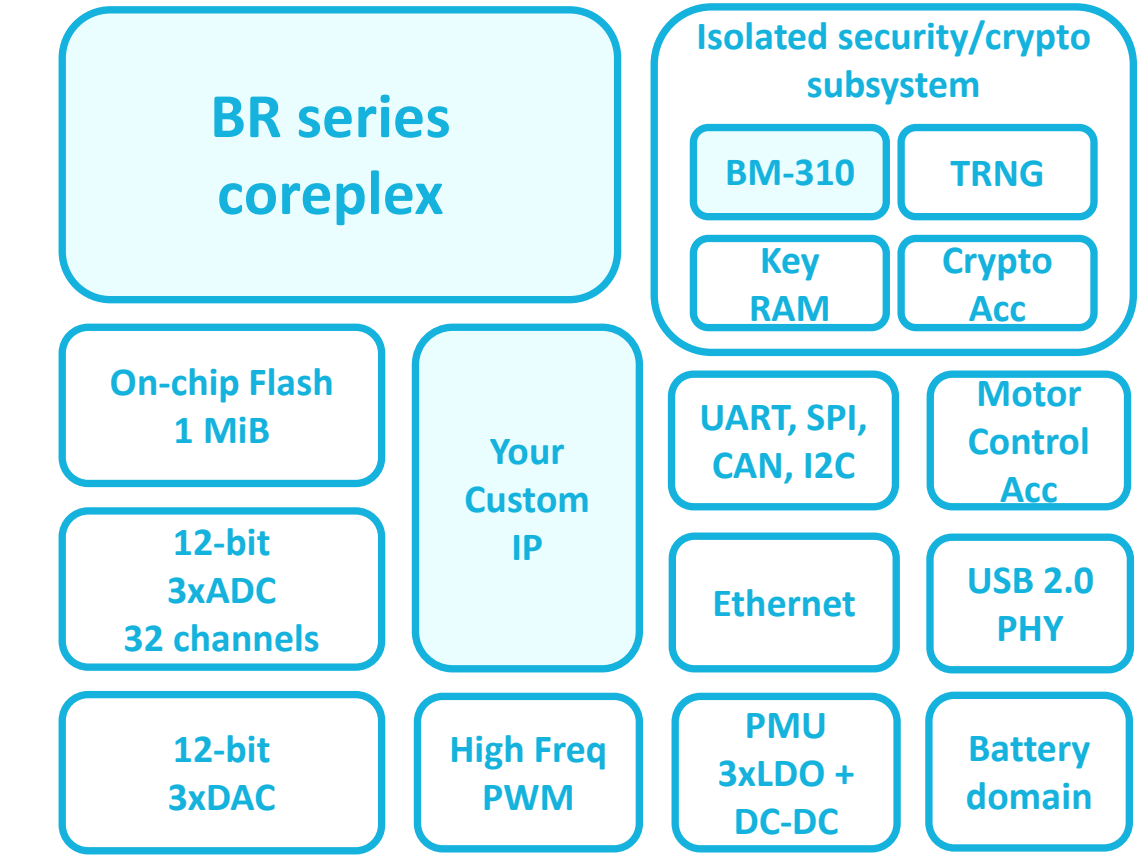
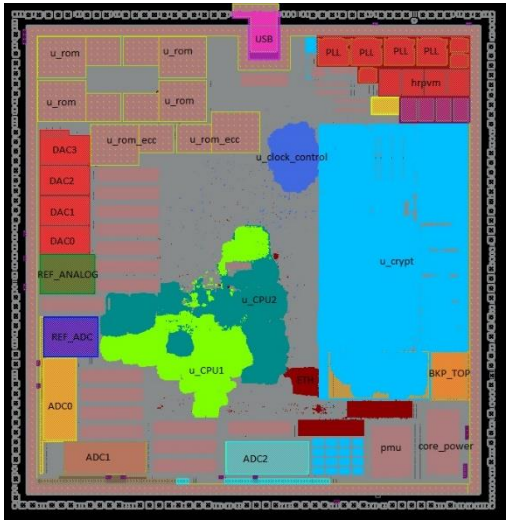


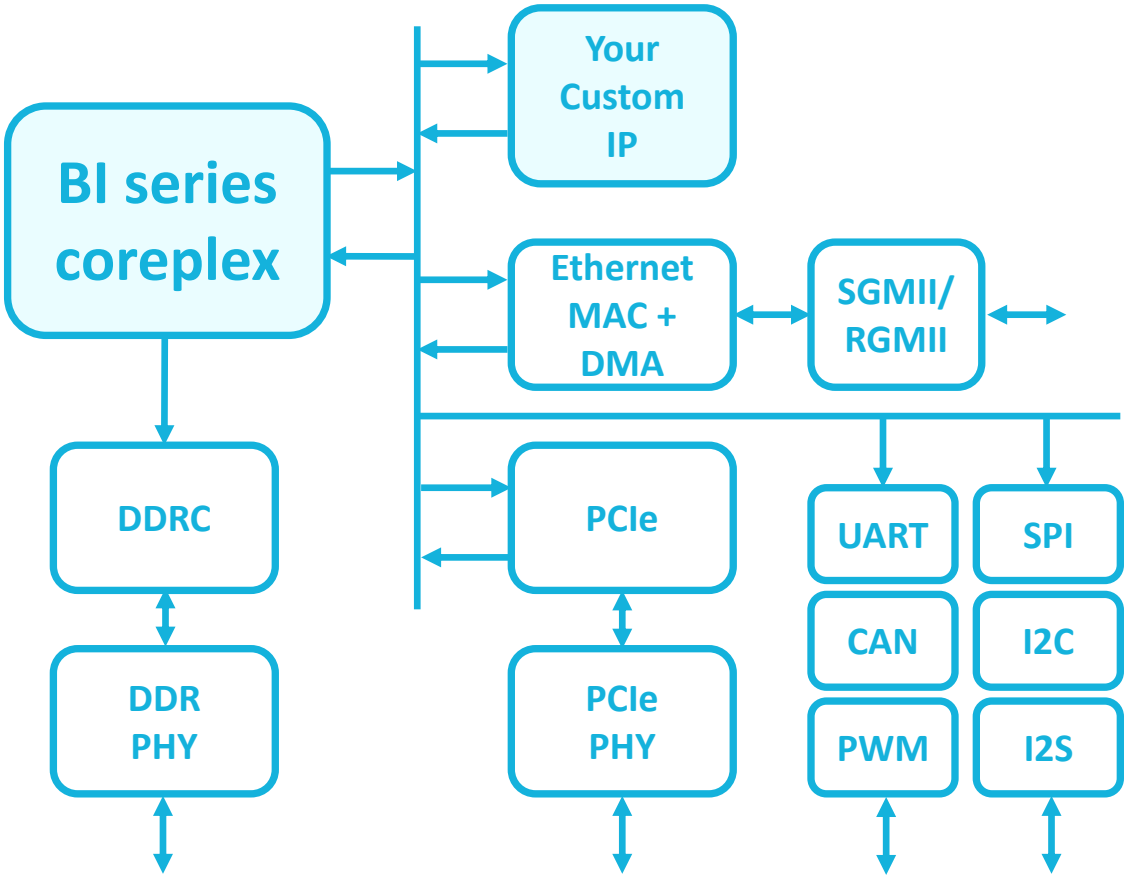
- TSMC 90nm LP

Milandr

- Motor control
- Predictive Maintenance
- Automotive
- Lock-step, fault-tolerant



Application processor platform



- TSMC 28nm
- TSMC 40nm

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- Pre-integrated platform with RISC-V application cores
- All SoC infrastructure included
- Targets
  - AI edge devices
  - Gateways
  - Industrial automation

BI series

Linux capable application cores

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BI-350

RV32IMAC[F]

32-bit Tiny Linux capable core targeting IoT applications

BI-651

RV64GC

64-bit Linux capable core targeting high performance in power constrained environment

BI-671

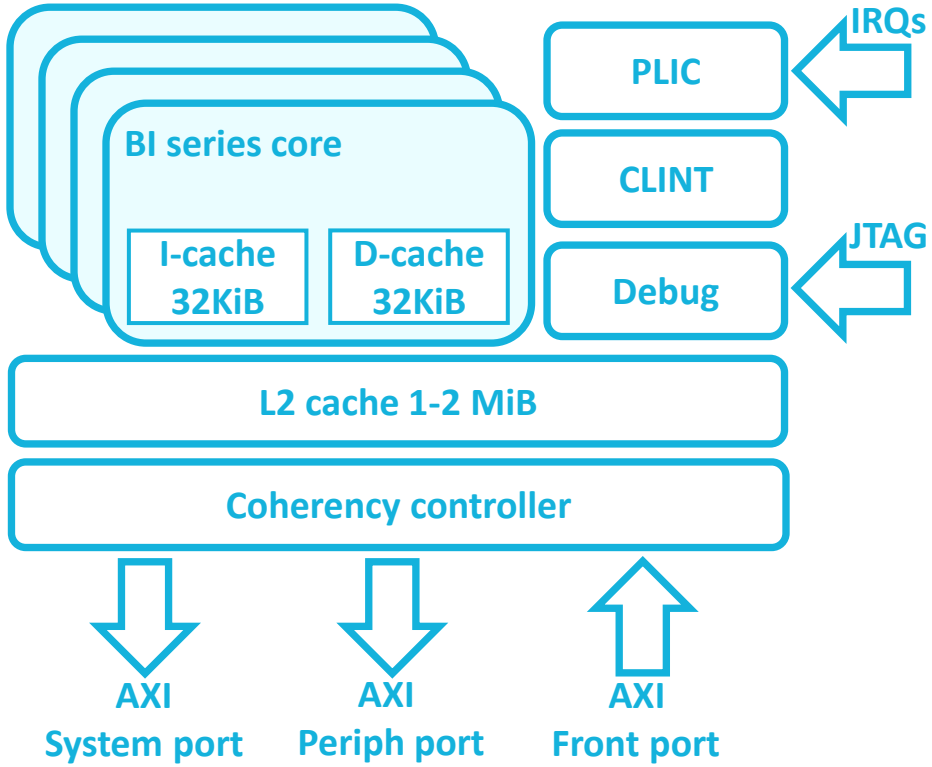
RV64GC

64-bit Mid-range application core for maximum single thread performance

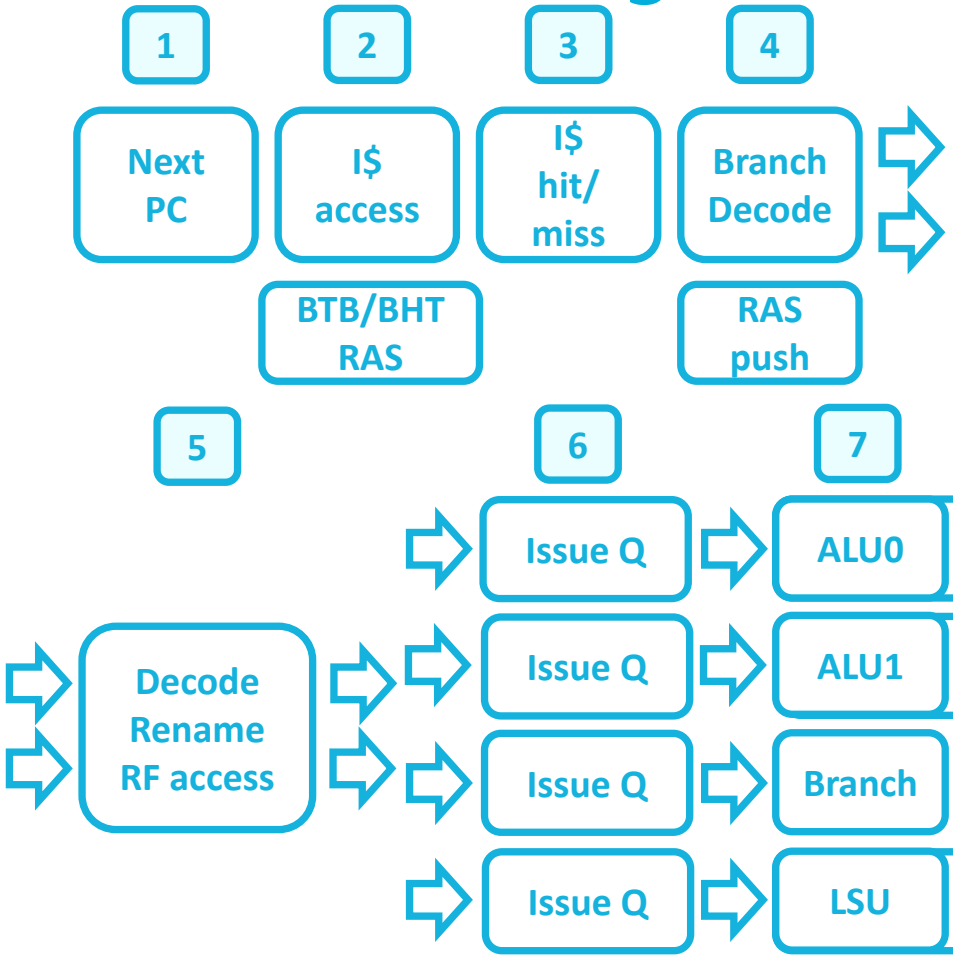
BI series core complex

Linux capable application cores

- RV64GC
- Multi-core fully coherent configuration
- Machine/User/Supervisor modes
- 32 KiB 8-way I/D caches
- L2 cache 1-2 MiB
- Debug module
- Platform Level Interrupt Controller
- Coherency controller for maintaining coherency with peripherals and accelerators



BI-671 mid-range OoO application core



- Mid-range performance
  - 2x comparing single-issue, 1.5x dual-issue designs
- Maximize power efficiency for given performance

BI-671 at a glance

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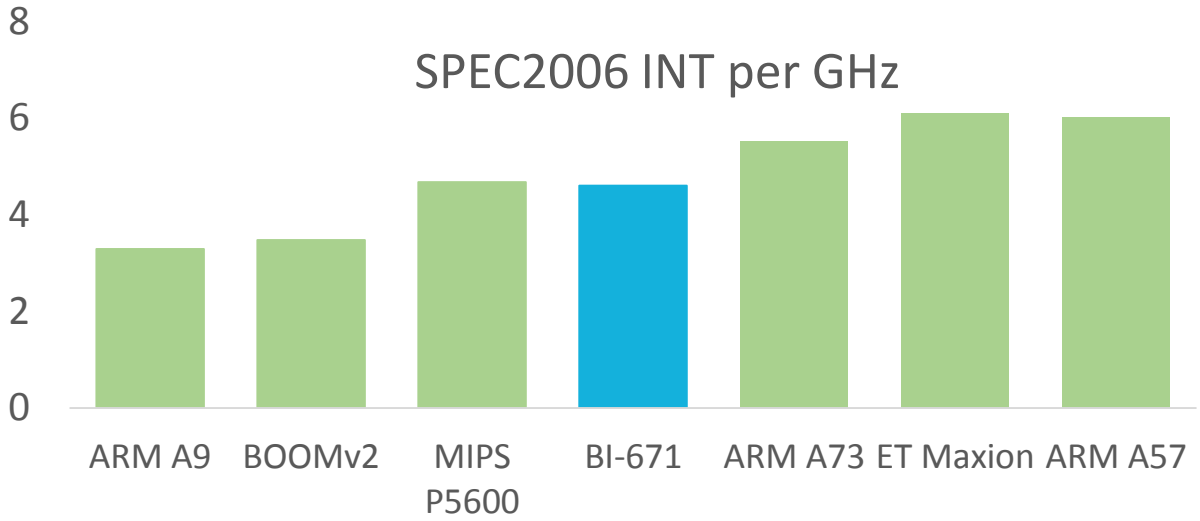
- 10 stage pipeline
- Fetch 8B per cycle
- Decode two instruction per cycle
- Reorder buffer 48 entries
- Load/Store queues 16 entries each
- 4R3W integer register file 64 entries
- I-TLB, D-TLB 16 entries each
- Hardware page walk 4 entries
- 4-way BTB 512 entries
- 8-way 32KiB L1 I- and D-caches
- Out-of-order issue
  - 2 ALUs, 1 Branch, 1 Load/Store, 1 FP

	TSMC 28HPC+, 12t
Frequency @ worst SSG	**1.2+ GHz**
Dual core + L2 1 MiB	**4.5-5 mm^2 ***

* including all necessary SRAMs

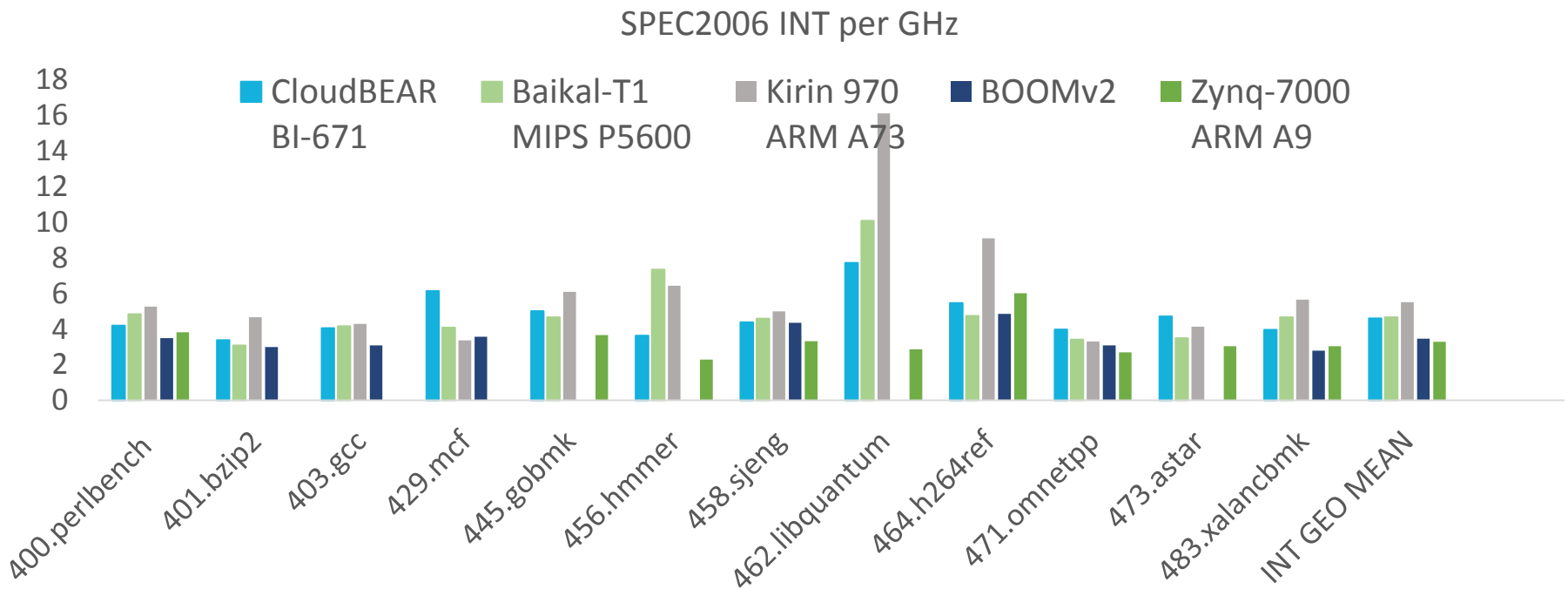
BI-671 at a glance



- 1.3-1.4x better performance than ARM A9 and BOOMv2
- On the same performance level with MIPS P5600
- 75-80% of ARM A73, ARM A57, ET Maxion performance

Benchmark	Score/MHz
Dhrystone	**3.58**
Coremark	**5.36**

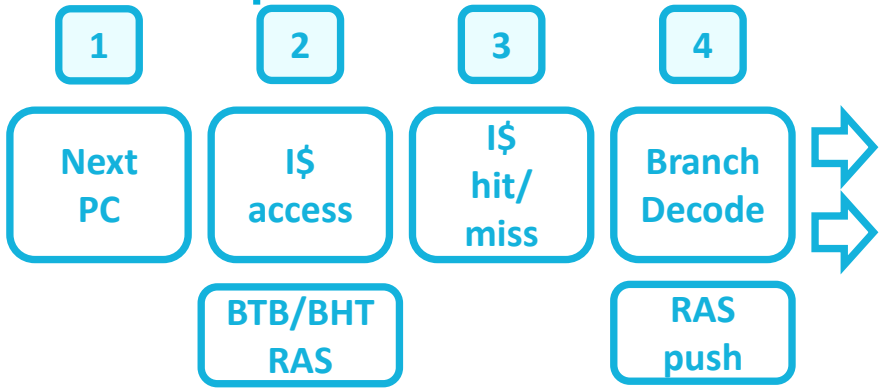
BI-671 SPEC2006 performance



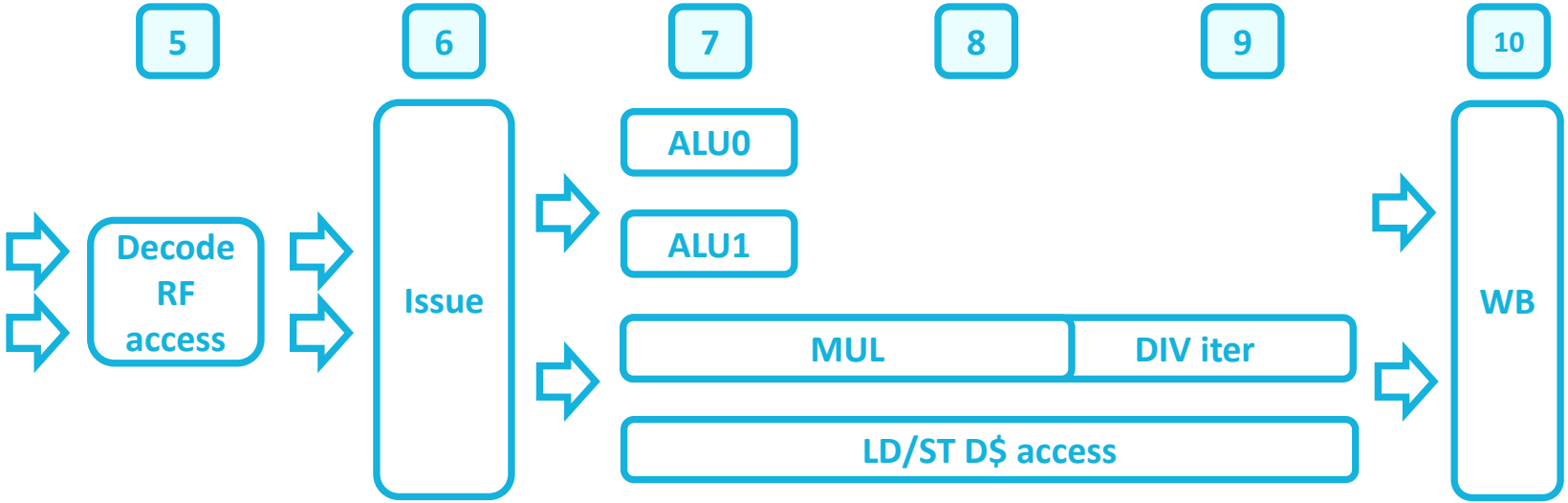
BI-671 data is preliminary and collected on FPGA prototype

bzip2, gcc, mcf – missing data for Zynq-7000 since require 2GiB RAM
gobmk, hmmer, libquantum, astar – missing data for BOOMv2

BI-651 power efficient application core



- Power efficient dual issue core
- High performance in power constrained Linux-capable devices



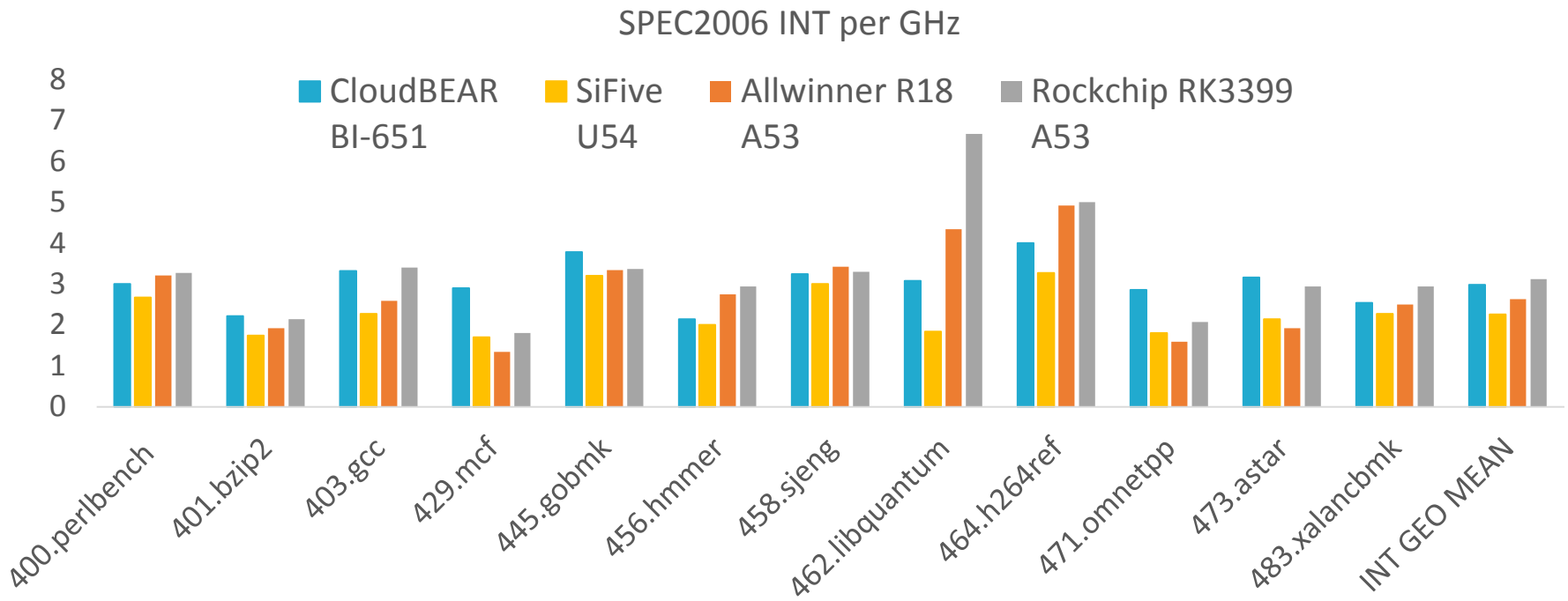
BI-651 performance

Dhrystone performance comparison	BI-651 BTB=512 BHT=2048 RAS=8	SweRV Late ALUs* off BTB=512 BHT=2048 RAS=8	SweRV Late ALUs on BTB=512 BHT=2048 RAS=8
GCC 8.2	2.44	2.10	2.36

Coremark performance comparison	BI-651 BTB=512 BHT=2048 RAS=8	SweRV Late ALUs* off BTB=512 BHT=2048 RAS=8	SweRV Late ALUs on BTB=512 BHT=2048 RAS=8
GCC 8.2	3.96	3.84	4.68
GCC 7.2	4.12	4.14	4.87

* Late ALU option was disabled for apple-to-apple comparison with SweRV core
BI-651 Late ALU option under implementation
Cycle-accurate simulation shows similar to SweRV Coremark performance

SPEC2006 BI-651

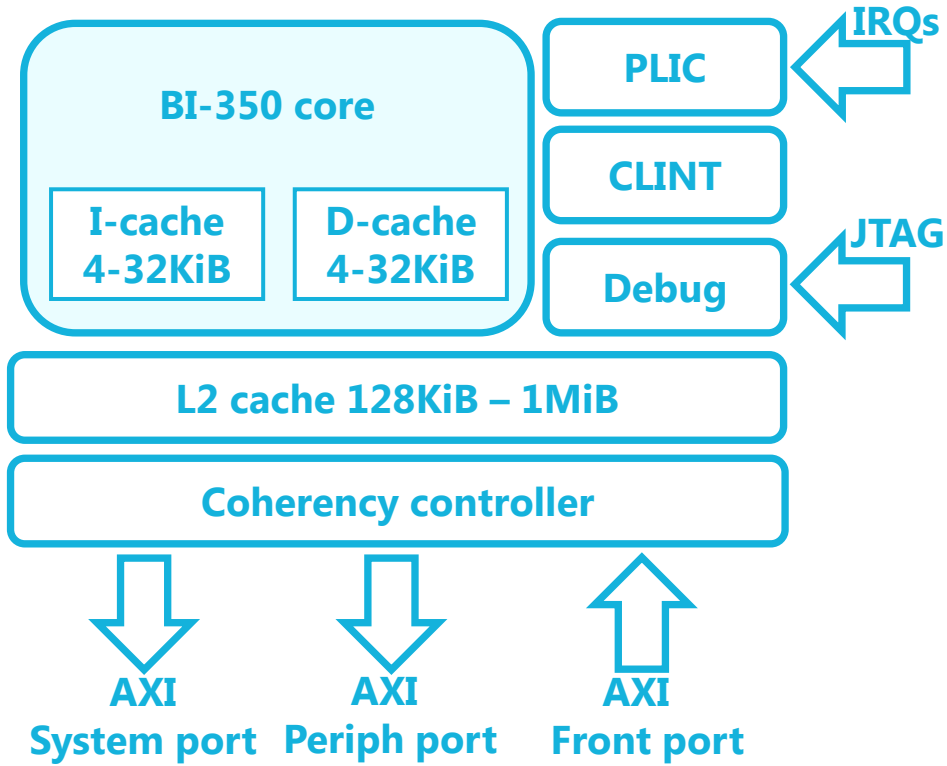


BI-651 data is preliminary and collected on FPGA prototype

BI-350 small Linux capable core

- Architecture: RV32IMAC[F]
- Single instruction issue
- Machine, Supervisor and User modes
- Configurable caches
  - Smaller size
  - Shorter cache line
  - Narrow memory interfaces
- L2 optional
- Tiny coherency controller configuration
- Configurable BTB, BHT, RAS

Benchmark	Score/MHz
Dhrystone	1.6
Coremark	2.9



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