Configurable LLDB Debuggers for RISC-V

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Who is Codasip

- The **leading provider** of RISC-V processor IP
  - Introduced their first RISC-V processor in November 2015
- Company founded in 2014 in the Czech Republic
  - Based on 10 years of university research on processor design automation
- Founding member of the RISC-V Foundation, [www.riscv.org](http://www.riscv.org)
- Now **Codasip GmbH**
  - Headquarters in Munich, Germany
  - R&D in Brno, Czech Republic
  - Office in Silicon Valley, US, and Shanghai, Pudong PRC
Codasip Bk

**Codasip Bk** = the Berkelium series, Codasip’s RISC-V processors

- Available immediately
- Pre-verified, tape-out quality IP
- Industry-standard interfaces
- Fully customizable

- **Bk3** – entry-level 32bit RISC-V Core
  - 3-stage single issue in-order pipeline
  - Very small, efficient design

- **Bk5** – 32bit and 64bit RISC-V Cores with Balanced Pipeline
  - 5-stage single issue in-order pipeline
  - Optional dynamic branch prediction
  - Optional cache memories

- **Bk7** – Linux-ready 64bit RISC-V Core
  - 7-stage single issue in-order pipeline with branch prediction
  - MMU for Linux
  - Cache memories (I$, D$)
RISC-V offers a wide range of ISA modules:

- I/E for integer instructions
- M for multiplication and division
- C for compact instruction
- F/D for floating point operations
- WIP: B, P, V, …

However, it may not be enough for your application domain or if you are looking for a key differentiator…

RISC-V allows custom extensions

SDK must be aware of the custom extensions

High level of automation needed

Codasip has tools for this task: Codasip Studio
What is Codasip Studio?

A unique collection of tools for **fast & easy modification** of RISC-V processors. **All-in-one**, highly automated. Introduced in 2014, **silicon-proven** by major vendors.

Customization of base instruction set:
- Single-cycle MAC
- Custom crypto functions
- And many more…

Complete IP package on output:
- C/C++ LLVM-based compiler
- C/C++ Libraries
- Assembler, disassembler, linker
- ISS (incl. cycle accurate), debugger, profiler
- UVM SystemVerilog testbench

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**Codasip Studio**

**CodAL** – processor description language

```plaintext
element i_mac {
  use reg as dst, src1, src2;
  assembly { "mac" dst ",", src1 ",", src2 };  
  binary { OP_MAC dst src1 src2 0:bit[9] };  
  semantics {
    rf[dst] += rf[src1] * rf[src2];
  };
}
```

Integrated processor development environment

- **RTL Automation**
- **Verilog**
- **VHDL**
- **SDK automation**
- **Verification Automation**
- **C/C++ LLVM-based compiler**
- **C/C++ Libraries**
- **Assembler, disassembler, linker**
- **ISS (incl. cycle accurate), debugger, profiler**
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Codasip GmbH
Bk Core Customization with Codasip Studio

Codasip Studio automatically generates all processor IP design kits and verifies for RISC-V compliance (you still need to verify your own resources and instructions).

ISA extensions are quickly implemented and analyzed during design space exploration.

Profiling of embedded application SW enables processor optimizations.
What is LLDB

- **LLDB** = open-source debugger built on libraries provided by LLVM and Clang
  - Clean architecture with easy-to-extend plugin system
  - Its own commands – mapping to gdb commands exists

- Part of SDKs

- Aware of custom instructions
  - Disassembly view and instruction stepping

- Works with ISS, RTL Simulators, and on-chip debugger
  - Using RSP protocol

- Codasip integrates LLVM 7.0.1 and 8.0.1 in its Studio
LLDB Architecture

- **Architecture definition**
  - In file `ArchSpec.[h/cpp]`
  - Specification of architecture (riscv32 and riscv64)

- **Plugin-based debugger**
  - **ABI**
    - Register definition, call frame info, function return objects, function calls, ...
  - **Platform**
    - Initialize and run IA/CA ISS
  - **Process**
    - Communication with IA/CA ISS
  - **Disassembler**
    - Enhancements that supports customizations
  - **Symbol File**
  - **Operating System**
  - ...
LLDB Interfaces

Command Line Interface (CLI)

```
$ lldb -q
```

Machine Interface (MI)
- Codasip-enhanced MI interface with added functionality (e.g. watchpoints)
Summary

Codasip is the leading provider of commercial-quality RISC-V IP

- Comprehensive off-the-shelf portfolio
  - From 32bit embedded to 64bit Linux-ready cores
  - Complete, fully verified IP packages
  - Available immediately
- Full-time, highly professional customer support staff

Codasip offers easy, automatized way to customize RISC-V

- Customization brings more performance, lower power/area, and differentiation
- Codasip provides a complete set of tools and resources to customize:
  - CodAL – C-like language for processor description
  - Codasip Studio – complete customization toolset
Thank you

Questions?