RISC-V Origins at Berkeley

- Krste’s group needed an ISA
- Originally for education
  - Teaching undergraduate courses
  - Research into custom processors
- ISA designed over four years
  - Feedback from building chips and software
- Long design cycle lead to a solid base ISA
Spinning Off from Berkeley

● Eventually we ended up with users
  ○ Surprised people were asking us to explain why the ISA was changing

● Led to forming two entities
  ○ RISC-V foundation, to shepherd the ISA specification
  ○ SiFive, to build RISC-V chips

● HiFive1 release late 2016
  ○ Announced at a RISC-V workshop

● Driver for embedded software
  ○ OpenOCD, GCC, Zephyr
Building the RISC-V Software Ecosystem

- People only pay attention when you have an ASIC
- HiFive Unleashed to bootstrap the RISC-V Linux software ecosystem
11 Software Talks at this Workshop
Software Implementations of RISC-V

- QEMU support RISC-V hosts and targets
  - Emulate RISC-V on an x86 host
  - Emulate x86 on a RISC-V host
Software Implementations of RISC-V

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“Enabling RISC-V Development with QEMU”
Wednesday at 10:15 am
Alistair Francis, Western Digital
C Compilers

- GNU-based toolchain is stable
  - Embedded since August, 2017
  - Linux since February, 2018

- LLVM is still experimental
  - Code generation for RV32 and RV64
C Compilers

GNU-based toolchain is stable
  - Embedded since August, 2017
  - Linux since February, 2018

LLVM is still experimental
  - Code generation for RV32 and RV64

“Open Source Compiler Tool Chains and Operating Systems for RISC-V”
Wednesday at 9:50 am
Jeremy Bennett, Embecosm
Debug and Trace

Olimex ARM-USB-TINY Probe

Digilent Arty FPGA

SiFive HiFive Unleashed & HiFive1 (FTDI)

PC (Debug Host)

Debug Translator
OpenOCD

or

Debug Translator
SEGGER J-Link

SiFive HiFive1 revB (J-Link OB)

SEGGER J-Link Probe
Debug and Trace

“Configurable LLDB Debuggers for RISC-V”
Wednesday at 5:15 pm
Zdenek Prikryl, Codasip
Debug and Trace

- Olimex ARM-USB-TINY Probe
- Digilent Arty FPGA
- SEGGER J-Link Probe
- PC (Debug Host)
- SiFive HiFive Unleashed
- HiFive1 revB (FTDI)

“SweRV (RISC-V) Debug, Trace and On-chip Analytics for SOC”
Wednesday at 1:05 pm
Sesibhushana Rao Bommana, Western Digital

“Configurable LLDB Debuggers for RISC-V”
Wednesday at 5:15 pm
Zdenek Prikryl, Codasip

SEGGER J-Link Probe
Commercial RISC-V Software Ecosystem

October 24, 2017

Lauterbach and SiFive Bring TRACE32 Support for High-Performance RISC-V Cores
Commercial RISC-V Software Ecosystem

October 24, 2017

Lauterbach and SiFive Bring TRACE32 Software for RISC-V High-Performance Cores

IAR EMBEDDED WORKBENCH FOR RISC-V NOW RELEASED

IAR Embedded Workbench offers excellent code optimizations for size and speed. As a well established frontrunner in the embedded industry you can rely on our tools to compile, analyze and debug your code beautifully.
Commercial RISC-V Software Ecosystem

October 24, 2017

Lauterbach and SEGGER Bring TRACE32 to RISC-V Support

The SEGGER Software Platform, including development tools, debug probes and middleware, provides a comprehensive one-stop solution for complete product development with microcontrollers based on the open RISC-V architecture. It simply works!

- Development Tools
- Debug Probes
- RTOS & Middleware

EMBEDDED WORKBENCH
RISC-V NOW RELEASED

Workbench offers excellent code optimizations for size and an established frontrunner in the embedded industry you can use to compile, analyze and debug your code beautifully.
Generating High Quality Code

“The SiFive 7 series cores have macro fusion support to convert a branch over a single instruction into a conditionally executed instruction.

This gives us about a 10% increase in CoreMark scores for this core.”

- Dhrystone and CoreMark still dominate
  - Dhrystone hasn’t changed since the 80’s
  - Both are synthetic benchmarks
- RISC-V has opened up innovation in embedded systems
- We need a new benchmark for the modern IOT
Generating High Quality Code

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“Embench”
Wednesday at 9:25 am
Dave Patterson
Languages Newer than C

- Go port can run Docker
  - Examples run on the HiFive Unleashed
- J extension working group
- Rust on RISC-V
Languages Newer than C

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- Rust on RISC-V

“Building Secure Systems using RISC-V and Rust”
Wednesday at 2:05 pm
Arun Thomas, Draper Labs
ISA vs Platform

- JTAG
- Debug Module
- Boot ROM
- Platform-Level Interrupt Control
- U54-MC Coreplex
- TileLink Switch
- TileLink Coherence Manager
- Banked L2$
- DDR3/4 ControllerPHY
- FU500 Base Platform
- ChipLink
- GbE
- OTP
- Mask ROM
- SD Card
- Quad SPI
- SPI
- I2C
- UART
- GPIO
- Clock Generation
- Clock/Reset Control

FPGA
- ChipLink
- TileLink Switch
- Your IP Block
- PCIe/USB/MIPI
ISA vs Platform

-Interrupt Controller
-Processor Core
-Cache Management
-DDR Initialization

Early Boot Flow
-Power, Clock, and Reset
ISA vs Platform

Processor Core

Interrupt Controller

Cache Management

DDR Initialization

Early Boot Flow

Power, Clock, and Reset

Platform Specification
Operating Systems

- **Freedom Metal, SiFive’s bare-metal embedded environment**
  - Bare-metal BSPs generated along with the hardware
  - Support for core RISC-V functionality, as well as SiFive blocks
- **Zephyr, a Linux Foundation RTOS**
- **OpenEmbedded, Debian, and Fedora**
Operating Systems

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“Open Source Compiler Tool Chains and Operating Systems for RISC-V”
Wednesday at 9:50 am
Mark Corbin, Embecosm
FreeRTOS
“Developing with FreeRTOS and RISC-V”  
Wednesday at 11:25 am  
Richard Barry, AWS
- Modern systems all require security
  - Secure boot
  - Trusted firmware
- RISC-V defines PMPs
- TEE working group
Modern systems all require security
- Secure boot
- Trusted firmware

RISC-V defines PMPs

TEE working group

"An open-source API proposal for a multi-domain RISC-V Trusted Execution Environment"

Wednesday at 3:20 pm
Cesare Garlati, Hex Five Security
Bootloaders for UNIX-Class Systems

- **Berkeley Boot Loader (BBL)**
  - Designed to boot university test chips
- **OpenSBI**
  - Clean implementation of SBI and early boot
- **u-boot**
  - Standard bootloader for embedded Linux systems
- **Coreboot**
  - First bootloader to add RISC-V support
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“OpenSBI Deep Dive”
Tuesday at 1:30 pm
Anup Patel, Western Digital
Linux Kernel

- Core RISC-V architecture support merged in early 2018
  - Runs on QEMU and HiFive Unleashed
- Most HiFive Unleashed drivers are posted for the next MW
- Upstream device tree bindings also posted for the next MW
  - Ready to begin integrating SOCs and boards
- BPF JIT was recently merged
- NOMMU port posted to the mailing list yesterday

77 unique contributors to arch/riscv/
Linux Kernel

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“Open Source Compiler Tool Chains and Operating Systems for RISC-V”
Wednesday at 9:50 am
Mark Corbin, Embecosm
- 64-bit glibc upstream since early 2018
- OpenEmbedded, Debian, and Fedora
Linux Userspace

- 64-bit glibc upstream since early 2018
- OpenEmbedded, Debian, and Fedora

“Enable RISC-V capability in cloud computing”
Wednesday at 11:50 am
Zhipeng Huang, Huawei
Getting Started

- **http://sifive.com/blog**
  - “Last Week in RISC-V”
- **sw-dev@groups.riscv.org**
- **#riscv on freenode**
- **Per-project mailing lists**
  - Most are upstream
  - linux-riscv@lists.infradead.org
  - linux-qemu@nongnu.org
  - binutils, GCC, glibc, GDB at FSF