Amazon Web Services (AWS) announces RISC-V Support in the FreeRTOS Kernel, enabling embedded developers to create IoT applications on the officially supported FreeRTOS kernel for microcontrollers – AWS 26 February 2019

Alibaba announces roadmap of RISC-V SoC from Embedded to Cloud CPUs – Alibaba. May 2019

SiFive Celebrates Historic 100 Design Wins Milestone – SiFive 6 June 2019

The EU Is Progressing With The Processor For A European Supercomputer
The Open Architecture RISC-V was chosen as the basis for the supercomputer, and the processor and platform developed with the European Processor Initiative (EPI) consortium. – TechNews. 5 June 2019

Western Digital releases their RISC-V Cores to the world... they will transition their consumption of silicon over to RISC-V, putting one Billion RISC-V cores per year into the marketplace – Hackaday. 13 February 2019

GreenWaves Technologies Named 2019 Cool Vendor in AI Semiconductors – Gartner 29 April 2019
New workloads demand processor flexibility for innovation

Legacy ISAs Are Decades Old

RISC-V Unlocks the Architecture & Enables Innovation

RISC-V is Open Source, transparent, and royalty free
Welcome to the RISC-V revolution!

- **RISC-V** is the open-source hardware Instruction Set Architecture (ISA)
- Frozen base user spec released in 2014, contributed, ratified, and openly published by the RISC-V Foundation

**The RISC-V Foundation** is a non-profit entity serving members and the industry

Our mission is to accelerate RISC-V adoption with shared benefit to the entire community of stakeholders.

- Drive progression of **ratified specs, compliance suite, and other technical deliverables**
- **Grow the overall ecosystem / membership**, promoting diversity while preventing fragmentation
- Deepen **community engagement and visibility**
RISC-V ushers in new era of silicon design

- Simple
- Stable
- Modular
- Clean Slate Design
- Designed for Extensibility / Specialization
More than 250 RISC-V Members in 28 Countries Around the World

RISC-V Foundation Growth History
September 2015 to May 2019

- 13 Universities
- 29 Consulting; Research
- 23 Development Tools; SW and Cloud
- 104 Individual RISC-V developers and advocates
- 51 Machine Learning/AI; Commercial Chip Vendors; FPGA; Broad Market; Networking; Application Processors, Graphics
- 45 Semiconductor IP; IP and Design Services; Foundry Services

May 2019
RISC-V is visibly disrupting the industry

1,183 attendees at 2018 RISC-V Summit

1,836 press articles

6,314 LinkedIn Followers

8,866 @RISC_V Twitter Followers

34,200+ articles mentioning RISC-V Foundation, member companies and ISA since January 2016
Programs increase member value + engagement

**Technical Deliverables**
- Guard against fragmentation
- Manage and progress technical deliverables through work groups and development team
- Process and initiate technical work groups
- Develop and manage member sandbox portal

**Compliance + Certification**
- Develop self serve testing and compliance certification suite
- Provide visibility to additional compliance certification and verification options

**Visibility**
- Drive constant drumbeat of member and foundation visibility through multiple media
- Engage in industry events and host Foundation events
- Cultivate strategic visibility through industry forums, analysts, and media

**Learning + Talent**
- Develop multi-level learning modules
- Connect universities, professors, and course material
- Develop badge and skill certification
- Match talent via online and event forums

**Advocacy + Outreach**
- Establish technical advocate program
- Engage geographic and domain specific engineers via advocate-led formal and informal opportunities
- Establish alliances with other organizations

**Marketplace**
- Provide online marketplace of providers and products
- Offer RFP matching to members
Engage!
Drive technical priorities in 20 focus areas

- Opcode Space Mgmt Standing Committee
- Software Standing Committee
- Base ISA Ratification Task Group
- Privileged ISA Spec Task Group
- UNIX-Class Platform Spec Task Group
- Formal Specification Task Group
- Trusted Execution Env Spec Task Group
- B Extension (Bit Manipulation) Task Group
- J Extension (Dynam. Translated Lang) Task Group
- P Extension (Packed-SIMD Inst) Task Group
- V Extension (Vector Ops) Task Group
- Cryptographic Extension Task Group
- Debug Specification Task Group
- Fast Interrupts Spec Task Group
- Memory Model Spec Task Group
- Processor Trace Spec Task Group
- Sv128 Specification Task Group
- Compliance Task Group
- Security Committee and proposed Safety Task Group
Come together. Right Now.
Meetups (1,500+ Members)

Bay Area RISC-V Group
https://www.meetup.com/Bay-Area-RISC-V-Meetup/

Rocky Mountain Area RISC-V Group
https://www.meetup.com/Rocky-Mountain-Area-RISC-V-Group/

Austin Area RISC-V Group
https://www.meetup.com/Austin-Area-RISC-V-Group/

Israel RISC-V Meetups
https://www.meetup.com/Israel-RISC-V-meetups/

Cambridge RISC-V Meetup Group

Bristol RISC-V Meetup Group
https://www.meetup.com/Bristol-RISC-V-Meetup-Group/

Pune RISC-V Group
https://www.meetup.com/Pune-RISC-V-Group/

Vienna RISC-V Meetup
https://www.meetup.com/Vienna-RISC-V-Meetup/

Shanghai RISC-V Meetup
https://www.meetup.com/shanghai-riscv/

San Diego RISC-V Group
https://www.meetup.com/San-Diego-RISC-V-Group/
Planning improved online marketplace of RISC-V offerings
Value Proposition for Members

- Ability to drive standards and set direction on future specifications
- Exposure to a large client base, across global markets
- Strong, growing ecosystem for collaboration
- Invested programs across technical areas and more to accelerate your strategy
- Several RISC-V Foundation groups for support (technical, marketing, educational, etc.)
- Use of the RISC-V trademarks and logos
RISC-V is already disrupting the silicon industry.

Thank you for driving us forward!

Join the Revolution
Get Social

@risc_v
risc-v-foundation
riscv.org
References


https://technews.bg/article-116996.html

