Compliance, Verification and Customization of RISC-V Cores and SoCs

Getting Started with RISC-V Roadshow
London, UK: September 26th 2019

© Imperas Software Ltd.
“nobody designs a chip without simulation”, at Imperas we believe that:

“nobody should develop embedded software without simulation”

Imperas develops simulators, tools, debuggers, modelling technology, and models to help embedded systems developers get their software running...

- and hardware developers get their designs correct

10+ years, self funded, profitable, UK based, team with much EDA (simulators, verification), processors, and embedded experience

www.imperas.com/riscv

www.OVPworld.org
Virtual Platforms Provide a Simulation Environment Such That the Software Does Not Know That It Is Not Running On Hardware

- The virtual platform is a set of instruction accurate models that reflect the hardware on which the software will execute
  - Could be 1 SoC, multiple SoCs, board, system; no physical limitations
- Run the executables compiled for the target hardware
- Models are typically written in C or SystemC
- Models for individual components – interrupt controller, UART, ethernet, ... – are connected just like in the hardware
- Peripheral components can be connected to the real world by using the host workstation resources: keyboard, mouse, screen, ethernet, USB, ...
- High performance: 200 – 500 million instructions per second typical, or boots Linux in <5 sec
Embedded Software Development, Debug & Test Tools

- Driven by unique SlipStreamer™ API to simulation engine
- Platform-centric 3Debug™ for debug of software on complex, heterogeneous platforms
- Verification, Analysis & Profiling (VAP) software tools
  - Non-intrusive: no modification of software or model source code
  - Users can easily define custom tools
- Tools at the appropriate and valuable levels of abstraction, granularity
  - Instruction tracing shows everything at lowest level of abstraction, no granularity
  - Function tracing and OS tracing show higher levels of abstraction
  - Instruction subset tracing, e.g. vector instructions or hardware virtualization, show finer granularity

“The Imperas virtual platform solutions for software development, debug and test, along with their open-source models, will help accelerate SoC and embedded software development for our customers.”

Charlie Hong-Men Su, Ph.D., Andes Technology CTO
Open Virtual Platforms (OVP) Library of High-Performance Processor Models

- Over 200 Fast Processor Models in OVP Library
- All models have both C and SystemC/TLM2 native interfaces
- ARM®: Models for ARMv4™, v5™, v6™, v7™ and v8™ architectures
- MIPS®: Models for microMIPS, MIPS32 and MIPS64 architectures
  - Verification, licensing, and distribution relationship
- Renesas: Models for RH850, V850 architectures; 16 bit microcontroller cores
- Synopsys (ARC): ARC6xx, ARC7xx, EM families
- RISC-V: RV32/64 IMAFDcen (2.2/2.3, 1.10/1.11 specs)
  - Envelope models (generic models of specification)
  - Vendor specific models: Andes, SiFive
  - Recent additional support: vector, bit manipulation instructions
- Altera Nios II
- Xilinx Microblaze

“OVP is addressing key issues in software development for embedded systems. By supporting the creation of virtual platforms, OVP is enabling early software development and helping expand the ARM user community.”

Noel Hurley, VP Business Development, ARM

"Imperas with its OVP Fast Processor Models is addressing key issues in software development for embedded systems. We are happy to work with Imperas to ensure that high quality models are easily available to our worldwide customers, helping them to develop and test software faster and more easily using virtual platforms."

Hirohiko Ono, senior manager of the MCU Tools Marketing Department, Renesas Electronics
Agenda

• Compliance and verification
• Customization
• Summary
Agenda

• Compliance and verification
  • Why is compliance important for RISC-V?
  • RISC-V compliance checking
  • Verification

• Customization

• Summary
Q: What is meant by “compliance”?  
A: The device works within the envelope of the agreed specifications

Q: Is there an easy process or path to follow to develop methodologies/tools for compliance?  
A: NO – all established ISAs are single company controlled and those companies work extremely hard on proprietary solutions to ensure that all designs that go out their door work correctly – so RISC-V has to pioneer compliance collectively

Q: What happens if the RISC-V industry builds devices that are not complying with specifications?  
A: Users cannot assume that tools like C compilers, operating systems, and application software will be transferable across devices and work correctly
The RISC-V Foundation’s Compliance Task Group

• Jun 2017 group started
  • Compliance testing is a testing technique which is done to validate whether the system developed meets the prescribed standards or not. It is **not design verification** testing
    • compliance testing is looking for issues like missing registers, modes, instructions – not for bugs in RTL implementations...
  • The tests have to be written to ensure compliance/non-compliance is **observable in a test signature**. The signatures are published so that the user does not have to run a reference model and can compare the results of their target runs to the reference signature

• Jan 2018 initial rv32i test suite provided by Codasip
• Jun 2018 Imperas, Embecosm worked on GitHub, made repo public
• Oct 2018 Imperas improved test coverage, added new suites, ported 32bit riscv-tests

© 2019 Imperas Software Ltd. September 2019
Imperas key contributor to the RISC-V Compliance Suite

• Compliance suite is ‘work in progress’

• Two components
  • Test suites
    • Each suite focuses on a feature set of the RISC-V envelope
    • Initial focus is instructions, user mode spec, e.g. rv32i, rv32im, rv32imc, rv64i, …
    • Awaiting RISC-V platform specifications to subset privilege spec, before starting privilege suites
  • Framework
    • Make, bash, and scripts
      • Encapsulate compiler tools, linkers, simulators, and targets (Devices Under Test)
    • Includes simulator: as example target, and to generate reference signatures
    • Run: Select suite and target
      • Runs each test, target produces signatures, compares to saved golden reference signature

• Available: www.github.com/riscv/riscv-compliance
Compliance Suite Status (rv32i)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Decode Coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>lb</td>
<td>100%</td>
</tr>
<tr>
<td>lh</td>
<td>100%</td>
</tr>
<tr>
<td>lw</td>
<td>100%</td>
</tr>
<tr>
<td>lbu</td>
<td>100%</td>
</tr>
<tr>
<td>lhu</td>
<td>100%</td>
</tr>
<tr>
<td>sb</td>
<td>100%</td>
</tr>
<tr>
<td>sh</td>
<td>100%</td>
</tr>
<tr>
<td>sw</td>
<td>100%</td>
</tr>
<tr>
<td>sl</td>
<td>100%</td>
</tr>
<tr>
<td>sll</td>
<td>100%</td>
</tr>
<tr>
<td>srl</td>
<td>100%</td>
</tr>
<tr>
<td>srlr</td>
<td>100%</td>
</tr>
<tr>
<td>sra</td>
<td>100%</td>
</tr>
<tr>
<td>srai</td>
<td>100%</td>
</tr>
<tr>
<td>add</td>
<td>100%</td>
</tr>
<tr>
<td>addi</td>
<td>100%</td>
</tr>
<tr>
<td>sub</td>
<td>100%</td>
</tr>
<tr>
<td>lui</td>
<td>100%</td>
</tr>
<tr>
<td>auipc</td>
<td>100%</td>
</tr>
<tr>
<td>xor</td>
<td>100%</td>
</tr>
<tr>
<td>xori</td>
<td>100%</td>
</tr>
<tr>
<td>or</td>
<td>100%</td>
</tr>
<tr>
<td>ori</td>
<td>100%</td>
</tr>
<tr>
<td>and</td>
<td>100%</td>
</tr>
<tr>
<td>andi</td>
<td>100%</td>
</tr>
<tr>
<td>slt</td>
<td>100%</td>
</tr>
<tr>
<td>sltu</td>
<td>100%</td>
</tr>
<tr>
<td>j</td>
<td>100%</td>
</tr>
<tr>
<td>jr</td>
<td>100%</td>
</tr>
<tr>
<td>lw</td>
<td>100%</td>
</tr>
</tbody>
</table>

Notes on rv32i test suite:
- 54 hand coded directed tests (average 150 instructions each)

Notes on Decode Coverage:
- Decode Coverage: observe changes on all bits of legal decodes
- Decode Coverage data from the Imperas Fault Simulation Coverage tool
  - ran 478,390 simulations in 308 secs

Similar status available on RV32IM, RV32IMC, RV64I, RV64IM suites

- Need more tests
- Investigate (more tests?)
- no tests yet (fence.i not in 2.3 RV32I)
- pseudos+CSR, no tests yet (not in 2.3 RV32I)
Coverage Metrics for Compliance Tests

- Coverage metrics used in RTL design verification are **not applicable** as they are often functional and connected to specific microarchitecture (RTL).

- Imperas’ Code Coverage Tool provides coverage of model source, which is useful to see how much of model is exercised by tests but **does not** show how much of specification is covered.

- Imperas’ Fault Simulation Coverage tool provides **Instruction Decode Coverage**:
  - explores the decodes of the instructions and mutates legal bits
  - detects that there is a test that stimulates & observes each bit
  - tool is very fast, runs in parallel, provides other metrics including data coverage
  - very useful for users as **provides coverage of custom instructions**
riscvOVPsim Simulator

- Instruction Accurate simulator using high performance Just-in-Time Code Morphing that executes RISC-V binaries and runs on Linux/Windows PC
  - Runs very fast, 1,000 MIPS
- Industrial quality for use in test development, software development, compliance testing and design verification
  - Includes capabilities to perform RISC-V compliance signature generation
- Maintained and supported by Imperas Software (www.imperas.com)
- Simulator restricted to single processor model and fully populated memory
- Includes Apache 2.0 Open Source model of complete RISC-V ISA envelope model of 2.2, 2.3, 1.10, 1.11 revisions of the RISC-V Foundation specifications
- FREE. No license keys or license management

Imperas riscvOVPsim Compliance Simulator
Issues to be sorted by RISC-V Foundation’s Compliance Working Group

- Detailed specifications needed
  - the structure of the Compliance Suite Framework (and how used)
  - what content of test should be (how written)
  - list of all the tests needed in each test suite (what is covered of specification)

- Formal process for RISC-V Foundation to allow user to claim their processor is a RISC-V processor
  - i.e. process to explore and record ‘is it a RISC-V compliant design?’
  - the ‘rubber stamp: RISC-V inside’
Imperas: Exploring Designs for Compliance

Note: these efforts/results are Imperas exploring designs brought into Imperas, not a discussion of what our customers are doing with our tools & test suites

• Many candidate DUTs (Device-Under-Test) = customers, partners, and for fun...
  • proprietary RTL, open source RTL
  • FPGA
  • Silicon
  • Simulators

• Process – goal is to load .elf file, run, write signature, compare with golden reference

• Develop encapsulation of DUT
  • So can run public GitHub Compliance Suite – and – Imperas internal compliance test suites

• Results of compliance checking
  • Missing registers
  • Missing instructions
  • Floating point mode change issues
  • PMP implementation issues
  • ...

September 2019
© 2019 Imperas Software Ltd.
RISC-V Processor & SoC Verification

• Two new issues in verification of SoCs based on open ISA processors:
  1. Verification of the processor
  2. Verification of the interface between the processor and the NoC/system bus

• New verification issues, as not a worry for Arm or MIPS based SoCs
• Can use many of the existing verification tools, but some new tools/models/flows are needed

• Minimum needed:
  • Reference model of the processor (OVP models available; can be customized)
  • Test generation
  • Processor instruction coverage measurement (Imperas tool available)
Google: open source riscv-dv instruction stream generator

Metrics: SystemVerilog design + UVM simulator for RTL

Imperas: model and simulation golden reference of RISC-V CPU
Agenda

• Compliance and verification
• Customization
  • Why customize the ISA?
  • How to add custom features
• Summary
There are and will be many different RISC-V CPU developers:

• Deliver RTL IP as a business (like Arm, MIPS, just for RISC-V)
  • e.g. Andes, CloudBear, Codasip, Incore, Syntacore, ...
• Develop internal cores for SoCs
  • e.g. Nvidia, ...
• Develop for internal use but make available as open source
  • e.g. Western Digital, ...
• Develop and use open source as a business opportunity
  • e.g. SiFive, ...
• Download and use open source RTL in their products
  • e.g. Greenwaves, Google, ...
• ...

© 2019 Imperas Software Ltd.
RISC-V CPU Adopters: (above & below the line)

New architectures (ML, IoT), arrays of processors, custom features, high performance, feature control (efficiency), large SoC design, architecture innovation, ...

Key requirement: ‘freedom to innovate’

Researchers, education, open source community, freely available, no license cost or restriction, ...

Key requirement: ‘free’
Many (above the line) adopters of RISC-V want to add their own custom extension instructions

- Traditional ISA choice has been hard if you want to add your own custom processor instructions to an ISA
- RISC-V as an open standard has specific regions of instruction decode space specifically allocated for users to add their own instructions

Challenges
- How to choose the processor IP starting point
- How to add instructions to processor RTL
- How to verify the complete RTL
- How to evaluate effectiveness and performance gains of new instructions
- How to enable software development utilizing the new instructions
Key Challenge of Optimizing Custom Instructions Requires New Methodology, Tools

• How to choose the processor IP starting point
• How to add instructions to processor RTL
• How to verify the complete RTL
• How to evaluate effectiveness and performance gains of new instructions
• How to enable software development utilizing the new instructions

➤ Extend instruction accurate simulation tools and models to support analysis and optimization of custom instructions
Agenda – Custom Instructions

• Who is adopting RISC-V and why...
• Adding custom instructions to RISC-V processors
• Custom instruction optimization flow
Custom Instruction Optimization Flow

• Show the flow used when designing new instructions to improve performance of applications running on a RISC-V processor
  • Allows evaluation and firming up of the instructions
  • Gets to the specification of the instructions needed to be implemented in RTL
• Introduce the technologies & tools needed for each stage

- Application software used for this walk-through is a character stream encoder, based on ChaCha20 encryption algorithm
  - Instruction Extensions to RISC-V courtesy of Cerberus Security Laboratories Ltd
  - https://cerberus-laboratories.com
Flow to add new custom instructions

1. Characterize C Application
2. Develop New Custom Instructions
3. Characterize New Instructions in Application
4. Optimize & Document model
5. Release & Deploy
The first thing needed is a simulator – think ISS, however …

- Simulator and model need to have ability to extend to allow custom instructions and new tools
- Ease of use also important
- Need to have a business-friendly open source license
Imperas Environment for Embedded Software Development, Debug & Test

Application Software & Operating System

Virtual Platform
- Peripheral
- Memory
- OVP CPU
- OVP CPU

JIT simulator engine

SlipStreamer API

Software Verification, Analysis & Profiling (VAP) tools
- Trace
- Profile
- Code coverage
- Memory monitor
- Protocol checker
- Assertion checkers

Multiprocessor / Multicore Debugger
- OS task tracing
- OS scheduler analysis
- Fault injection
- Function tracing
- Variable tracing
- ...

Eclipse IDE

© 2019 Imperas Software Ltd. September 2019
Flow to add new custom instructions

Characterize C Application

- Instruction Accurate Simulation
- Trace / Debug
- Timing Simulation
- Function Timing / Profiling
Instruction Accurate simulation of C application

- Cross compiled C application targeting RV32IM
  - Character stream encoder, with ChaCha20 encryption algorithm
- IA simulation
  - Imperas RISC-V ISS with configurable model of RISC-V specification selecting RV32IM
- Semihosting
  - Enables bare metal application to very simply access host I/O
- runs fast
  - Over 1 billion instructions a second (standard PC)
  - Linux and Windows supported host OS
Cycle Approximate simulation C application

- Same C application
- IA simulation + timing Estimation (IA+E)
  - Includes annotated timing estimation for RV32IM processor
- Same simulation data results, different timing as now counting cycles
- Shows how long algorithm will take to execute

- Extends simulated time
  - Was 12.89 secs now takes 16.59 secs
Function Profile C Application

- Same C application
- IA+E simulation
- Sampled profiling with call stack analysis

- Shows proportion of time spent in each application function
  - 21.35% spent in processLine
Flow to add new custom instructions

Characterize C Application
- Instruction Accurate Simulation
- Trace / Debug
- Timing Simulation
- Function Timing / Profiling

Develop New Custom Instructions
- Design Instructions
- Add to Application
- Add to Model
- Add Timing
Add custom instructions to application

- Inline assembly using new instructions replacing C code
- 4 new instructions
- Cross Compile using standard tool
- Run on IA simulator

Unimplemented instruction exception
- As the instructions have not yet been added to the simulator model
Add custom instructions to model

- Use standard Open Virtual Platforms (OVP) instruction modeling APIs to add new instructions (and optional state) as **new extension library**
  - Easy to extend decode table, add efficient behavioral JIT code
  - Optionally can call directly into user’s provided C function of behavior
- Compile and link model extension library
- Simulate IA with ISS plus standard model extended with new library

➤ Instruction count and simulated time have reduced (IA)
Cycle Approximate simulation including custom instructions

- IA simulation + timing annotation + custom instructions
  - Includes timing estimation for RV32IM processor
  - Need to add timing estimation for new custom instructions
- Simulate using C code application with inline assembler of custom extensions
- IA simulator + timing tool + custom extension instruction library

- See estimated improvement in throughput of application on new processor
  - Was 16.59 secs without custom instructions
  - **Now 9.21 secs with custom instructions**
Trace custom instructions

- Simulator has many trace features built in
- See new custom instructions in trace disassembly
- Can select when/where to turn trace on/off
  - Very efficient tracing
Debug custom instructions

• Imperas MPD is Eclipse based source code debug tool
• Can debug using source line or instruction level
• See new custom instructions and any new additional state registers
Function Profile custom instructions application

- IA simulation + timing annotation + custom instructions with sampled profiling

- Shows where slowest function is
  - Now much faster...

- Shows benefits of using custom instructions
  - processLine was 21.35% now 16.3%
Basic Block (BB) Profile custom instructions application

- IA simulation + timing annotation + custom instructions with detailed BB profiling
- Shows where expensive instruction sequences are
- Allows understanding of instruction performance
  - Useful for Compiler teams
  - Useful for Hardware teams
Flow to add new custom instructions

Characterize C Application
- Instruction Accurate Simulation
- Trace / Debug
- Timing Simulation
- Function Timing / Profiling

Develop New Custom Instructions
- Design Instructions
- Add to Application
- Add to Model
- Add Timing

Characterize New Instructions in Application
- Instruction Accurate Simulation
- Trace / Debug
- Timing Simulation
- Function Timing / Profiling
Flow to add new custom instructions

Characterize C Application
- Instruction Accurate Simulation
- Trace / Debug
- Timing Simulation
- Function Timing / Profiling

Develop New Custom Instructions
- Design Instructions
- Add to Application
- Add to Model
- Add Timing

Characterize New Instructions in Application
- Instruction Accurate Simulation
- Trace / Debug
- Timing Simulation
- Function Timing / Profiling

Optimize & Document model
- Instruction Coverage
- Line Coverage
- Instruction Performance
- Generate PDF model doc
Further tools for model developers

• Model source line coverage
  • To see how completely the tests exercise the model
Further tools for model developers (2)

- **Custom instruction coverage**
  - To see that there are tests for new instructions

- **Custom instruction profile**
  - See how long the simulator takes to execute each instruction
  - Use to focus speed up simulation of instructions
  - Enables improvement of speed of simulation runs
Document custom instructions

• Imperas tools automatically generate a processor model document PDF
• Includes all base model registers and any new registers
• Provides detailed documentation of new custom instructions

Chapter 2

Instruction Extensions

RISC-V processors may add various custom extensions to the basic RISC-V architecture. This processor has been extended, using an extension library, to add several instruction using the Custom0 opcode.

2.1 Custom Instructions

This model includes four ChaCha20 acceleration instructions (one for each rotate distance) are added to encode the XOR and ROTATE parts of the quarter rounds.

2.1.1 chaCha20p1

<table>
<thead>
<tr>
<th>000000</th>
<th>Rx2</th>
<th>Rdi</th>
<th>000 (QQ)</th>
<th>Rdi</th>
<th>Custom0 0000011</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
</tr>
<tr>
<td>0 16</td>
<td>0 15</td>
<td>0 14</td>
<td>0 13</td>
<td>0 12</td>
<td>0 11</td>
</tr>
</tbody>
</table>

dst = (src1 src2) <<<16

2.1.2 chaCha20p2

<table>
<thead>
<tr>
<th>000000</th>
<th>Rx2</th>
<th>Rdi</th>
<th>001 (QQR)</th>
<th>Rdi</th>
<th>Custom0 0000011</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
</tr>
<tr>
<td>16 0</td>
<td>15 0</td>
<td>14 0</td>
<td>13 0</td>
<td>12 0</td>
<td>11 0</td>
</tr>
</tbody>
</table>

dst = (src1 src2) <<<12

2.1.3 chaCha20p3

<table>
<thead>
<tr>
<th>000000</th>
<th>Rx2</th>
<th>Rdi</th>
<th>010 (QRR)</th>
<th>Rdi</th>
<th>Custom0 0000011</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
</tr>
<tr>
<td>0 8</td>
<td>7 6</td>
<td>5 4</td>
<td>3 2</td>
<td>1 0</td>
<td>0 0</td>
</tr>
</tbody>
</table>

dst = (src1 src2) <<<8
Flow to add new custom instructions

Characterize C Application
- Instruction Accurate Simulation
- Trace / Debug
- Timing Simulation
- Function Timing / Profiling

Develop New Custom Instructions
- Design Instructions
- Add to Application
- Add to Model
- Add Timing

Characterize New Instructions in Application
- Instruction Accurate Simulation
- Trace / Debug
- Timing Simulation
- Function Timing / Profiling

Release & Deploy
- Check RISC-V Compliance
- Use as reference for RTL Design Verification
- Use in Imperas/OVP Platforms, EPKs
  - Heterogeneous / Homogeneous
  - Multi-core, Many-core
- Imperas Multi-Processor Debug, VAP tools
- Port OS, RTOS (Linux, FreeRTOS...)
- Use in many simulation envs (inc. SystemC)
- Deliver to end users

Optimize & Document model
- Instruction Coverage
- Line Coverage
- Instruction Performance
- Generate PDF model doc

(© 2019 Imperas Software Ltd.)
Demo: Boot Linux on Virtual Platform of SiFive FU540

- ~7 seconds to the Linux prompt
- Eclipse-based eGui for debug
  - Platform-centric debug with visibility into all processors and peripherals, and event-based debug
- Running Verification, Analysis and Profiling (VAP) tools, including OS-aware tools
  - Drill down from OS task tracing to function tracing to line tracing to instruction tracing

© 2019 Imperas Software Ltd.
Summary

- Verification & Compliance are a new challenge for open ISAs
- Additional verification tasks related to the open ISA processor
- Custom instructions are a key value proposition of RISC-V
  - Adding custom instructions requires solving the key challenge of how to optimize those instructions
- Instruction accurate (IA) simulation environment using IA models can be extended to enable custom instruction analysis and optimization
- Flow for optimizing custom instructions in RISC-V processors is being used in real designs
Thank You

• Visit www.imperas.com/riscv and www.OVPworld.org/riscv for more information

• RISC-V Foundation Compliance Suite, includes riscvOVPsim available:
  • https://github.com/riscv/riscv-compliance

Kevin McDermott
VP Marketing, Imperas Software
kevinm@imperas.com