Embedded Software Development for RISC-V Based SoC
MINRES Technologies GmbH

- MINRES is an enabling company, dedicated to providing the expertise and solutions required for improving embedded software development productivity
- MINRES Technologies GmbH is privately-held and based in Munich
- For more information visit www.minres.com or mail to info@minres.com
Embedded design impact

- Huge variety of applications with different requirements
- Often "invisible", but provide essential functionality
- Extensibility is important
- Domain specific requirements
  - For example functional safety based on ISO26262
RISCV challenges and opportunities I

- RISCV scales well; not only up, but also down
  - Area and power efficiency
  - Functional safety elements can be added

- Extensibility in application specific scenarios
  - Addressing limited resources
  - Security needs

- Business model
  - Can replace in house solutions
RISCV challenges and opportunities II

- RISCV can drive better proliferation of embedded systems
- SW needs driving more and more HW requirements
  - Alignment is essential in order to tap into that potential
- Tools + IPs + knowledge
HW/ SW development process

- HW and SW are developed within different flows
- Integration often reveals issues
- Availability and observability of HW
RISCV SW ecosystem

- Good support of standard SW tools
  - Compiler (gcc toolchain, llvm)
  - Multiple ISS implementations (Qemu, Spike, DBT-Rise-RISCV)
  - Tracing (Lauterbach, Segger)

- How do I ensure my SW works on my target HW?
  - HW is a system of components which interact

- How do I ensure to be done in time?
Pressing productivity challenges

- Development process transparency
- Limitations of the target and its use
  - System accessibility
  - System visibility and control
  - Scalability
Agile embedded software development methods enabled by Virtual Prototypes/Platforms
MINRES offerings

- Know-how in system modeling, VP implementation and embedded SW development
  - Educational services
  - Methodology services
  - Design consulting services

- Open-source productivity IP
  - SystemC Components Library: [git.minres.com/SystemC/SystemC-Components](git.minres.com/SystemC/SystemC-Components)
Early embedded SW development

- **Shift-left to shorten time to market**
  - Start SW development even before having RTL or silicon
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VP based methodology allows to start early
Efficient VP development

- Single sourcing and code generation
- Productivity libraries
  - e.g. SystemC components library
- Instrumentation for debugging aids
  - logging, tracing, transaction recording
DBT-RISE based Implementation Flow

- **Core Specification**
  - Core DSL
    - RISC-V: ~ 500 LOC
  - Generated C++
    - RV32IMAC: ~ 6k LOC
  - Target specific C++
    - RV32IMAC: ~ 1.5k LOC
- **DBT-RISE**
  - ~ 5k LOC
- **Platform Spec.**
  - RDL 300 LOC
  - SystemC Platform Model
  - SystemC Register stubs
- **DBT-RISE ISS**
- **HiFive1**
  - GDB Adapter
  - SERVER
  - ADAPTER
  - VM
  - ARCH
  - UART
  - GPIO
  - SPI
  - PWM
  - RAM
  - PLIC
- **system environment/test bench**

**Core Specification Details**
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Debug & analysis in FW/SW development

- Comprehensive analysis, visibility, tracing, and debug possibilities
- Non-intrusive observation and debugging of behavior
- Tools to fuse HW and FW/SW events to ease debugging system behavior
Modern SW development practices

- Continuous integration for VP and embedded SW
- Test driven design
- allow for agile methodologies
Beyond VP use cases

- VP model must be early, but can become basis for other models during design process
  - Adding timing information allows architectural analysis
  - Can deliver use case information for other components
  - Can be used in verification environment for reference information
Approximated timing for communication

SW or derived information is important for performance analysis

Even larger system components can be integrated
Links to verification

- Pin accurate in SystemC
  - Adapter between transactions and pin level
- Verification effort
- Bridging multiple abstraction levels introduces need for interpretation
Summary

Our mission is to champion and facilitate changes that improve embedded software development productivity.

Visit www.minres.com and the open source projects on git.minres.com or github.com/minres
BACKUP
RISCV events

- We plan to establish RISCV meetup in collaboration with interested parties in Munich
- If interested to participate or contribute, please contact:
  - info@minres.com