RISC-V SoC FPGA Brings Real-Time to Linux
Microchip’s FPGA Strategy
To be the leading provider of programmable RISC-V solutions

Open. Lowest Power. Programmable RISC-V Solutions

- Highly differentiated, open ISA alternative to Arm® technology
- AMP Mode: Simultaneous Linux + Real-Time Flexibility
- Enhances our low power position
- Enhances our security position
- Provenance enables full transparency for trusted design
- A lower cost ASIC migration path than Arm

Key RISC-V Foundation and Industry Partnerships

- Microchip Foundation Board Member: Ted Speers
- Microchip Working Committee Members: Stuart Hoad, Richard Newell
- Strategic Partnership with
  - Soft 32-bit uCs, Hard Quad-core 64-bit uPs + uC
  - Common MSS architecture, boards, ecosystem
## CPUs: Mi-V Soft CPUs & Roadmap

<table>
<thead>
<tr>
<th>Core</th>
<th>LE's</th>
<th>CoreMark</th>
<th>Cache</th>
<th>Mul/Div</th>
<th>Floating Point</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mi_V_RV32IMA_L1_AHB</td>
<td>10K</td>
<td>2.01</td>
<td>8K I and D</td>
<td>Yes</td>
<td>N/A</td>
<td>Now</td>
</tr>
<tr>
<td>Mi_V_RV32IMAF_L1_AHB</td>
<td>26K</td>
<td>2.01</td>
<td>8K I and D</td>
<td>Yes</td>
<td>Single Precision</td>
<td>Now</td>
</tr>
<tr>
<td>Mi_V_RV32I_AHB</td>
<td>5K</td>
<td>-</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>CQ4’19</td>
</tr>
<tr>
<td>Mi_V_RV32IMA_L1_AXI</td>
<td>10K</td>
<td>2.01</td>
<td>8K I and D</td>
<td>Yes</td>
<td>N/A</td>
<td>Now</td>
</tr>
</tbody>
</table>

- **Mi_V_RV32I_AHB**
  - Small core, with/without debug, 5K LEs

- **Mi_V_RV32IMA_L1_AHB with SECED available**

**Legend:**
- Mi-V = Mi-V RISC-V Ecosystem
- RV32I = 32 bit integer machine
- M = Multiply and Divide
- A = Atomic Instructions
- F = Single Precision Floating Point
- D = Double Precision Floating Point
- C = Compressed Instructions
- L1 = Instruction and Data Cache
- AHB = AHB Bus Interface
- AXI = AXI Bus Interface
SoftConsole Eclipse IDE

- A single tool chain for RISC-V and Arm MCUs
  - Easy migration from Arm to RISC-V
- Running on Linux or Windows Hosts
- Bundled with example projects and Real-Time Operating Systems (RTOSs)
Why RISC-V for a SoC FPGA?

- The RISC-V ISA is Open. Open ISA’s allow for …
  - Low cost migration to ASICs, royaltyfree usage
  - Innovation for custom architectures – free “architectural license” doesn’t restrict usage to fixed architectures

- The RISC-V ISA is simple. Simplicity …
  - Allows for a low-power implementation
  - Lowers cost of ownership - easier to learn, customize and debug
  - Simple architectures are easier to secure against threats

Open, Lowest Power, Cost Optimized, Programmable SoC
PolarFire® SoC Architecture

Open, Lowest Power, Cost-Optimized, Programmable SoC
Lowest Power Mid-Range FPGAs

- **10G Bridging & Aggregation**
- **Video & Image Processing**
- **Portable Communications**
- **RF and Baseband Signal Processing**
- **Packet Processing & Traffic Management**
- **Low-Power Optics**

**Control Plane (PCIe, GigE, 10GE)**

**Hardware Acceleration**
Mid-Range FPGA Landscape

PolarFire FPGAs deliver 30 to 50% lower power than competing SRAM-based mid-range FPGAs

Only cost and power optimized FPGA with 12.7G SERDES
- Power/cost decrease from mid-range FPGAs
- Performance upgrade from cost/power optimized FPGAs

High Density FPGAs

Competing Mid-range FPGAs

Competing Low Density FPGAs

Transceiver Rate

28G+

10G

5G

Relative Power & Cost

COST / POWER OPTIMIZED

PERFORMANCE OPTIMIZED

Microchip
Lowest Power – Save Up to 50%

- Enabling Application Performance at Significantly Lower Power
  - Static power 10x Reduction
  - Transceiver 2x Reduction

- Total power up to 50% lower than best case competitor number
- PolarFire Customer: $1.5/W in BOM cost saving due to power savings
Security is All About Layers

To protect your information you need Secure Hardware, Design Security and Data Security

Information Assurance:
Key storage using Physically Unclonable Function (PUF) Advanced Crypto Accelerators Licensed Patent Protected DPA Resistance Pass through License

Anti-Tamper: Secure Bitstream, Tamper Detection, Active Mesh, No Copying, Cloning, or Reverse Engineering

Microsemi FPGAs provide a strong foundation for your security needs

“Some call cybercrime the greatest transfer of wealth in human history” – The Center of Strategic and International Studies, July 2013, The Economic Impact of Cybercrime

“The number of IoT sensors is expected to approach 30 billion in 5 years – and each unit is a potential entry point for cyber-criminals” – The Economist Intelligence Unit, 4/11/2016

The DPA logo is a trademark of Cryptography Research, Inc. used under license
Exceptional Reliability

- Error Free SEU immune Fabric Configuration
  - No need to detect configuration errors
    - No scrubbing required
    - No triple mode redundancy needed
    - Lowers cost

- Memories are also protected
  - Built-in SECDED on 33-bit word

- System Controller Suspend Mode for Safety-Critical Applications

SEU a growing concern for equipment demanding 99.999% uptime
## PolarFire Product Family

### FPGA Fabric

<table>
<thead>
<tr>
<th>Features</th>
<th>MPF100</th>
<th>MPF200</th>
<th>MPF300</th>
<th>MPF500</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Elements (4LUT + DFF)</td>
<td>109K</td>
<td>192K</td>
<td>300K</td>
<td>481K</td>
</tr>
<tr>
<td>Math Blocks (18x18 MACC)</td>
<td>336</td>
<td>588</td>
<td>924</td>
<td>1480</td>
</tr>
<tr>
<td>LSRAM Blocks (20 kbit)</td>
<td>352</td>
<td>616</td>
<td>952</td>
<td>1520</td>
</tr>
<tr>
<td>uSRAM Blocks (64x12)</td>
<td>1008</td>
<td>1764</td>
<td>2772</td>
<td>4440</td>
</tr>
<tr>
<td>Total RAM (Mbits)</td>
<td>7.6 Mbits</td>
<td>13.3 Mbits</td>
<td>20.6 Mbits</td>
<td>33 Mbits</td>
</tr>
<tr>
<td>uPROM (kbits)</td>
<td>297 Kbits</td>
<td>297 Kbits</td>
<td>459 Kbits</td>
<td>513 Kbits</td>
</tr>
<tr>
<td>User DLL’s/PLL’s</td>
<td>8 each</td>
<td>8 each</td>
<td>8 each</td>
<td>8 each</td>
</tr>
</tbody>
</table>

### High Speed I/O

- 250 Mbps - 12.7 Gbps Transceiver Lanes
  - 8
  - 16
  - 24

- PCIe Gen2 Endpoints/Root Ports
  - 2
  - 2
  - 2

### Total I/O

- Total User I/O
  - 284
  - 364
  - 512
  - 584

### Packaging

<table>
<thead>
<tr>
<th>Type / Size / Pitch</th>
<th>Total User I/O (HSIO / GPIO)</th>
<th>GPIO CDRs / XCVRs</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC32G325 (11x11, 11x14.5*, 0.5 mm)</td>
<td>170(84/86) 8/4*</td>
<td>388(156/232) 16/16</td>
</tr>
<tr>
<td>FC32G525 (16x16, 0.5 mm)</td>
<td>300(120/180) 15/4</td>
<td>388(156/232) 20/16</td>
</tr>
<tr>
<td>FC32V484 (19x19, 0.8 mm)</td>
<td>284(120/164) 14/4</td>
<td>512(276/236) 24/16</td>
</tr>
<tr>
<td>FC32G484 (23x23, 1.0 mm)</td>
<td>244(96/148) 13/8</td>
<td>584(324/260) 24/24</td>
</tr>
<tr>
<td>FC32G784 (29x29, 1.0 mm)</td>
<td>364(132/232) 20/16</td>
<td></td>
</tr>
<tr>
<td>FC32G1152 (35x35, 1.0 mm)</td>
<td>512(276/236) 24/16</td>
<td></td>
</tr>
</tbody>
</table>

*Addtional Temp Grade: Military (-55°C-125°C) - Leaded packages only

Note: FC484M package is a lidded package whereas the FCG484I package is not.

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**Extended Commercial (0°C-100°C) and Industrial (-40°C-100°C) Temperature Support for all Die Package Combinations - RoHS only**
PolarFire® SoC Architecture

Open, Lowest Power, Cost-Optimized, Programmable SoC
Enabling Purpose-built, Real-time, Low Power systems

Safety Critical Systems

Imaging and Machine Learning

Collaborative Robots

Industrial IoT

Secure Communications and Portable Embedded Systems

Smart Weapons, Drones and UAVs
Real-time Linux?

- Widespread Linux adoption
  - Rich OS with thousands of applications to choose from

- Requirements still exist for real-time while running Linux
  - Safety-critical
    - The ability to deterministically monitor the execution environment
  - Real-time system control
    - Completing tasks deterministically, on time every time
  - Securing the IoT
    - Execute a trusted execution environment deterministically for consistent results

- Working with our partner
  - We have been able to architect a complex SoC FPGA that provides determinism and a rich OS within the same multi-core CPU cluster
Variable Execution Time in Typical Application Processors

- Periodic Interrupts
  - $T_0 = T_1$
- Inconsistent Execution Times
  - $E_0 \neq E_1 \neq E_2$

Branch predictors, cache misses and lack of coherency affect determinism negatively.
Real-Time and Linux

- Turn off the CPU branch predictors
- Convert L1 to Tightly Integrated Memory
- Make sure all cores coherent to the memory subsystem
- Make the memory system deterministic
- Share coherent memory for message passing

RESULT
No Execution Time Variability

| 5723600 | E51 RT BP Off | U54 SMP 1 | U54 SMP 2 | U54 SMP 3 | U54 SMP 4 |
| 5723100 |
| 5722600 |

Direct Access
Coherent Buffers
L2
DDR4
PolarFire SoC - RISC-V Enabled Innovation Platform

Freedom to Innovate in

- Linux and Real-Time
- Thermal and Power Constrained Systems
- Securely Connected IoT systems
- High-Rel Safety Critical Systems

SiFive

ultrasoc
Low Power: RISC-V MSS vs. Alternatives

- **Low Power MSS**
  - Low power RISC-V micro-architecture
  - 2MB L2 cache: increases cache hit/miss ratio
  - 0.5-0.9W lower power

- **LTE Digital Front End Application**
  - 3-7W lower power for 60MHz 4x4 MIMO implementation
PolarFire® SoC inherits best-in-class PolarFire FPGA Security
- DPA-resistant bitstream programming
- Anti-tamper
- Cryptographical bound supply chain assurance
- Physically unclonable function
- True random number generator
- Side channel resistant crypto coprocessor

PolarFire SoC has:
+ Secure Boot
+ Spectre and Meltdown immunity
+ Physical memory protection
+ SECDED on all memories
Freedom to Start Software Development

Eclipse IDE Design Flow

- Free Rapid Software Development and Debug Capabilities Without Hardware
- Complete PolarFire SoC Processor Subsystem Model
- Available now
Freedom to Begin Hardware Development

PolarFire SoC Embedded Experts Development Kit

HiFive Unleashed Expansion Board + HiFive Unleashed Development Board = MPFS-DEV-KIT
PolarFire® FPGA Award-Winning Features

- 30-50% lower power over competitive devices
- Defense-grade security
- Exceptional reliability
- Smallest, lowest power, secure form factors – 11x11, 16x16, 19x19

PolarFire Microprocessor Subsystem

- Linux and real time in a deterministic, coherent CPU cluster
- 30-50% lower power
- Defense-grade secure boot
- Spectre/Meltdown immune
- SECDED on all memories

Click here to learn more
Thank You