Unshackling Memory!

Martin Fink
Forward-Looking Statements
Safe Harbor | Disclaimers

This presentation contains forward-looking statements that involve risks and uncertainties, including, but not limited to, statements regarding our contributions to and proposals for the RISC-V ecosystem, technology and product development, business strategies and growth opportunities, the capabilities and features of our RISC-V cores, expectations regarding data growth and its drivers, and industry trends. Forward-looking statements should not be read as a guarantee of future performance or results, and will not necessarily be accurate indications of the times at, or by, which such performance or results will be achieved, if at all. Forward-looking statements are subject to risks and uncertainties that could cause actual performance or results to differ materially from those expressed in or suggested by the forward-looking statements.

Key risks and uncertainties include volatility in global economic conditions; business conditions and growth in the storage ecosystem; unexpected advances in competing technologies; our development and introduction of products based on new technologies and expansion into new data storage markets; the impact of competitive products and pricing; actions by competitors; risks associated with acquisitions, mergers and joint ventures; difficulties or delays in manufacturing; and other risks and uncertainties listed in the company’s filings with the Securities and Exchange Commission (the “SEC”) and available on the SEC’s website at www.sec.gov, including our most recently filed periodic report, to which your attention is directed. We do not undertake any obligation to publicly update or revise any forward-looking statement, whether as a result of new information, future developments or otherwise, except as required by law.
Agenda

RISC-V: FROM THEN TO NOW

PROCESSING CHALLENGES

WESTERN DIGITAL RISC-V INNOVATIONS

WHAT’S NEXT
Incredible Growth!
Western Digital’s RISC-V History & Vision

Innovating through open standards

Select RISC-V open-source innovations, strategic partnerships and investments only.

2015

Join as Platinum member

Explore RISC-V solutions

2019

Create Data Centric Architectures

Ship 1B cores

- SweRV Core™ EH1
- PlatformIO Partnership
- Fedora®Linux®
- QEMU
- Abstraction Layer Firmware
- SweRV ISS™
- Code Density
- SBI
- OmniXtend™

Select RISC-V open-source innovations, strategic partnerships and investments only.

Western Digital

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Agenda

RISC-V: FROM THEN TO NOW

PROCESSING CHALLENGES

WESTERN DIGITAL RISC-V INNOVATIONS

WHAT’S NEXT
Issues with Processing Today:

Legacy architectures are stifling innovation

Surging development costs
Why Settle for Legacy Architecture?

• Not easily extensible
  – Solving future problems requires more diverse solutions

• Old assumptions limit innovation
  – Main memory controlled by the CPU
  – Homogeneous processors are best
Hardware Development Costs Growing Exponentially

Source from IBS Research via https://www.extremetech.com/computing/272096-3nm-process-node
We’ve Seen this Play Out Before

Untenable costs drove open-source software
Hardware Development now Requires

INNOVATION + COLLABORATION

Open hardware development being fueled by economics
A robust ecosystem is critical
Agenda

1. RISC-V: FROM THEN TO NOW
2. PROCESSING CHALLENGES
3. WESTERN DIGITAL RISC-V INNOVATIONS
4. WHAT’S NEXT
Cache Coherent Memory Fabric – OmniXtend

Memory Fabric

RISC-V

Other CPU

GPU

AI Accelerator

FPGA

Network Fabric

Data is at the center of the architecture
Why OmniXtend

<table>
<thead>
<tr>
<th>Interface</th>
<th>Physical I/O</th>
<th>Connection</th>
<th>Standard Coherence?</th>
<th>Reference Design</th>
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<tbody>
<tr>
<td>CCIX</td>
<td>PCIe</td>
<td>Point to Point</td>
<td>Yes</td>
<td>No</td>
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<tr>
<td>Gen Z</td>
<td>Custom</td>
<td>P2P, Switched, Fabric</td>
<td>Yes</td>
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<td>CXL</td>
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<td>Point to Point</td>
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<td>Partial</td>
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<tr>
<td>Open CAPI</td>
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<td>Ethernet</td>
<td>Fabric, P2P</td>
<td>Open</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Only Ethernet based fabric that supports cache coherency and is open
OmniXtend Well-Positioned for Growth

Open-source collaboration to drive development

**FUTURE WORK TO BE DONE IN CHIPS ALLIANCE**
Open to all organizations

**OMNIXTEND REFERENCE DESIGN**
Allegro files available now in CHIPS Alliance
https://github.com/chipsalliance/omnixtend
Western Digital Embedded SweRV

SWERV CORE EH1 WAS THE FIRST STEP TO REPLACE A PROPRIETARY CORE

- Needed more IPC
- Smaller size with specific I/O capabilities

SWERV CORE UPDATES NOW IN CHIPS ALLIANCE

https://github.com/chipsalliance/Cores-SweRV
Western Digital SweRV Announcement

TAPPING OUT OUR FIRST SOC BASED ON SWERV CORE EH1

CODASIP WILL SUPPORT COMMERCIAL ADOPTION OF SWERV
http://www.codasip.com/swerv
Additional Processing Requirements

Multiple processors used in many embedded applications
With many I/O calls, a multi-threaded, embedded core could replace two CPUs

Very small cores are used to replace state machines and sequence logic
Need a low power, very small core with good performance
New SweRV Cores
In CHIPS Alliance Github

The first commercial embedded, dual threaded core: SweRV Core EH2

An ultra small, moderate performance, 4 stage pipeline core: SweRV Core EL2

6.3 Coremarks/Mhz*

3.6 Coremarks/Mhz*

*Simulated performance based on internal testing.
Contribution Recap

OmniXtend
- In CHIPS Alliance
- Reference Design

SweRV Core EH1
- First SoC taping out
- Codasip support

SweRV Core EH2 & EL2
- First commercial dual threaded, embedded core
- Smaller performance core

Demonstrated Progress toward 1B cores and Data Centric Solutions
Agenda

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PROCESSING CHALLENGES

WESTERN DIGITAL RISC-V INNOVATIONS

WHAT’S NEXT
What’s Next

UNSHACKLING MEMORY FROM THE PROCESSOR

LEVERAGING RISC-V AND OPEN SOURCE HARDWARE

EXECUTING OUR RISC-V ROADMAP

CONTINUE TO CONTRIBUTE TO THE ECOSYSTEM
THE UPRISING OF
RISC-V®

DATE  12.10.2019
TIME  6:30 PM - 9:30 PM
PLACE  THE TECH INTERACTIVE

WE ARE CELEBRATING THE DRAMATIC GROWTH
AND INNOVATION BROUGHT FORTH BY RISC-V.
IT IS ALREADY A MAJOR MOVEMENT AND GROWING
INTO THE FUTURE. THIS PARTY IS SPONSORED BY
MICROCHIP, SIFIVE AND WESTERN DIGITAL.