Open-source computing

A new blueprint for microprocessors challenges the industry’s giants

*RISC-V is an alternative to proprietary designs*

“Your Own RISC”

By Hal Hodson
MISSION

UNLEASH YOUR ROADMAP

BUILD YOUR CUSTOM SILICON

VIBRANT ECOSYSTEM
## Processor IP Showcase

**Tomorrow @ 2:20pm**

**Grand Ballroom 220-A**

### 2 Series
- Power & area optimized
- 2–3-stage single-issue pipeline

### 3/5 Series
- Efficient performance
- 5–6-stage single-issue pipeline

### 7 Series
- High performance
- 8-stage, dual-issue superscalar pipeline

### 8 Series
- Maximum performance
- 3-wide 12-stage out-of-order superscalar pipeline

### U Cores
- 64-bit application cores
- Linux, datacenter, network baseband

### U5 Series
- Linux-capable application processors
- Compare to Cortex-A35

### U7 Series
- High performance Linux capable processors
- Compare to Cortex-A55, A55 MP4

### U8 Series
- Highest performance application processors
- u84 Standard Core
- Compare to Cortex-A72

### S Cores
- 64-bit embedded
- Storage, AR/VR, machine learning

### S2 Series
- Area-optimized 64-bit microcontrollers
- S21 Standard Core
- No Arm equivalent

### S3 Series
- S31, S36 Standard Cores
- Compare to Cortex-R5, R5F

### S7 Series
- S76, S76-MC Standard Cores
- Compare to Cortex-R8

### E Cores
- 32-bit embedded
- MCU, edge computing, AI, IoT

### E2 Series
- Our smallest, most efficient cores
- E20, E21, E24 Standard Cores
- Compare to Cortex-M0+, M4, M4F

### E3 Series
- Balanced performance and efficiency
- E31, E34 Standard Cores
- Compare to Cortex-R5, R5F

### E7 Series
- High performance 32-bit embedded cores
- E76, E76-MC Standard Cores
- Compare to Cortex-M7
SiFive U8-Series

The World’s First RISC-V Out-of-Order Processor Core IP

1.5X  2X

Performance Per Watt\(^1\)  Area Efficiency\(^2\)

See Endnote For Details
The Open Secure Platform Architecture of SiFive Shield

Today @ 2:20pm
Grand Ballroom 220-C
The Open Secure Platform Architecture of SiFive Shield
Today @ 2:20pm
Grand Ballroom 220-C

Pre-integrated, Verified, and Delivered with SiFive Core IP
Introducing Scalable New Core IP for Mission Critical Use

Today @ 3:40pm

Grand Ballroom 220-B
The SiFive Vector Processor
Tomorrow @ 1:20pm
Grand Ballroom 220-B
Enabling Security with AWS Qualified IoT Devices
Tomorrow @ 4:10pm
Grand Ballroom 220-B

GET A FREE SIFIVE LEARN INVENTOR*

*Limited Supply
SiFive Software Solutions

Scalable software solutions to meet the demands of vastly configurable IP

RISC-V Software State Of The Union
Tomorrow @ 12:50pm
Grand Ballroom 220-C
Growing SiFive Ecosystem
Thank You

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FOOTNOTES:

1 – Based on SiFive internal estimates of SPEC Int/GHz per Watt, and Power per mm² of SiFive U84 Core with L2$ in 16nm vs Competitor Core estimates of core implementation in 16nm.

2 – Based on SiFive internal estimates compared to SiFive U7-Series using iso-process & iso-frequency methodology.