A Leading Provider of Microcontroller, Security, Mixed-Signal, Analog & Flash-IP Solutions

Getting Started with PolarFire® SoC and Renode
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Tuesday Dec. 10, 2019
Agenda

- Getting Started with Libero SoC v12.3
- Using Renode for PolarFire® SoC Designs
Getting Started with Libero SoC v12.3

- www.microsemi.com/liberosoc

- Create a PolarFire SoC Project with an EAP license

- Libero SoC v12.3 released today!

- Libero SoC v12.0: Software Tool of the Year – 2019 WEAA
Welcome to Microsemi's Libero® SoC v12.3

Libero SoC v12.3 offers high productivity with its comprehensive, easy to learn, easy to adopt development tools for designing with Microsemi's power efficient flash FPGAs, Soc FPGAs, and Rad-Tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v12.3 for designing with Microsemi's RTG4 Rad-Tolerant FPGAs, SmartFusion®2 and IGLOO® 2 SoC FPGAs, and PolarFire FPGAs.

To design with Microsemi’s older Flash FPGA families, use Libero SoC v11.9 and subsequent service packs.

What's New in Libero SoC v12.3
Clocks tab:
Set MSS clock frequency
Select clock source
Set reference frequency
Getting Started with Libero SoC v12.3

Fabric Interface Controllers:

FIC 0 AXI4
- Master
- Slave

FIC 1 AXI4
- Master
- Slave

FIC 2 AXI4
- Slave

FIC 3 APB
- Master

Information Classification: General
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IO Configurations Available:

- eMMC
- USB
- SD/SDIO
- GEM0 / 1
- QSPI
- SPI_0 / 1
- MMUART_0 / 1 / 2 / 3 / 4
- I2C_0 / 1
- CAN_0 / 1
- GPIO_0 / 1 / 2
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The “Image” tab highlights IOs in use and their configurations.
# Getting Started with Libero SoC v12.3

## PolarFireSoC MSS System (Pre-production) Configurator

<table>
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<tr>
<th>Microsemi:SgCore:PFSOC_MSS:1.0.100</th>
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## Table

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<th>Clocks</th>
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<th>IO Configuration</th>
<th>DDR Topology</th>
<th>DDR Memory Initialization</th>
<th>DDR Memory Timing</th>
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⚠️ Question mark indicates a missing or unclear part of the diagram.

Information Classification: General
Debug Trace:
Expose UltraSoC Debug pins to the fabric

JTAG:
Expose fabric JTAG debug pins

Interrupt:
Expose 64 interrupt pins to the fabric
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CLK & Reset

Debug

APB Master

IRQ Generating Timer

PF SoC MSS
Currently Available:

- Synthesis
- Place and Route
- Timing Verification
Getting Started with Renode

Anton Krug
Use SoftConsole 6.2 to target PolarFire® SoC
  - Eclipse based IDE for developing for RISC-V and Arm® (Cortex®-M) bare-metal targets
  - [https://www.microsemi.com/softconsole](https://www.microsemi.com/softconsole)

Do not have silicon at the moment...?

...Renode to the rescue!
  - Antmicro’s simulator targets various platforms
  - Bundled with SoftConsole since 5.3 release
  - Single GDB connection to all cores (beta)
Bundled Examples

- FreeRTOS - WebServer
  - Use host’s tools
    - wireshark, ping, web-browsers and development/testing frameworks
  - I call it: hexdump on steroids
    - Compressing payloads to fraction of their original size is useful on resource constrained targets
Bundled Examples Cont.

- Julia example
  - We had a bit of fun
  - Modeling an FPGA peripheral
    - Contains performance tricks

- Cyril Jean’s talk at 2:50 p.m. in 220-B
- Renode training tutorials
C# Modeling of the FPGA Fabric

- Bundled models (MSS and others)
- Heavily object oriented
  - In long term is great, but has learning curve
- A lot of functionality is inherited
  - UART in 27 lines, video adapter in 175 lines
- Can make very versatile models
- Answer what-if questions quickly
C, Python and Verilog

- C# is the primary preference for the models
- C, Python and Verilog (Verilator) can be also used
- However missing the C# Infrastructure
- Not validating spec of your peripheral as thoroughly
- Out-of-the-box experience will improve in the future
CI and CT

- Docker containers on the Docker hub
  - Contains full SoftConsole, toolchains, Renode and Robot
    - Able to build projects and run tests automatically
    - Builds all projects and configurations with very few arguments
    - Headless or interactive, can run on every single commit
    - RISC-V toolchain is bundled with 40 arch/abi multilibs
      - good for experiments
  - Will work well on internal servers or in the cloud
Thank You

Any Questions?