SweRV Cores Roadmap

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Agenda

• Western Digital and RISC-V history

• SweRV Cores roadmap and CHIPS Alliance

• SweRV EH1 core recap:
  – Architecture and microarchitecture
  – Performance

• SweRV EH2 and EL2 cores:
  – Microarchitecture
  – Performance
  – Simultaneous multi-threading examples
  – Implementation areas

• RISC-V Flash Controller Vision

• Conclusions
Western Digital RISC-V History

Motivated by our desire for open standard interfaces

Platinum member

Explore RISC-V solutions

Announce plans to ship 1B cores

Contribute to Fedora Linux® & Arduino Cinco ports

Contribute SweRV™ Core EH1, PlatformIO, OmniXtend™, SBI, QEMU...

2015  2016  2017  2018  2019
Open source RISC-V cores

- SweRV EH1 core addresses high performance embedded requirements, increasing performance to 4.9 CM/MHz while keeping size in 0.1 mm² range at 28 nm TSMC. SweRV EH2 introduces multi-threading, while EL2 represents ultra-low power core for variety of SoC applications.
RISC-V Cores roadmap

CPU technology roadmap

SweRV™ EH1
SweRV EH1: 32-bit, 9-stage, 2-issue
800 MHz 28 nm TSMC
0.11 mm²

SweRV™ EH2
SweRV EH2: 2-threads, 9-stage, 2-issue
1.2 GHz 16 nm TSMC
0.067 mm²

SweRV™ EL2
SweRV EL2: small 4-stage core, 1-issue
600 MHz, 16 nm TSMC
0.023 mm²

https://github.com/chipsalliance/Cores-SweRV

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## SweRV EH1 core recap

[https://github.com/chipsalliance/Cores-SweRV](https://github.com/chipsalliance/Cores-SweRV)

- **8 stage pipeline**
  - Fetch to commit
- **3 stall points**
- **Execution pipes**
  - ALU ops statically assigned to I0, I1 pipes
  - ALU's are symmetric
- **Load/store pipe**
  - Load-to-use of 2
- **Multiply pipe**
  - 3 cycle latency
- **Divide pipe**
  - Up to 34 cycles, out-of-pipe
- **Coremark score of 4.9 CM/MHz**

### 8 stage pipeline diagram

<table>
<thead>
<tr>
<th>Load/Store Pipe</th>
<th>I0 pipe</th>
<th>I1 pipe</th>
<th>Multiply Pipe</th>
<th>Divider</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC1</td>
<td>EX1 adder</td>
<td>EX1 adder</td>
<td>M1</td>
<td>34 cycle, out-of-pipe</td>
</tr>
<tr>
<td>DC2</td>
<td>EX2</td>
<td>EX2</td>
<td>M2</td>
<td></td>
</tr>
<tr>
<td>DC3 Load result</td>
<td>EX3</td>
<td>EX3</td>
<td>M3 Mult Result</td>
<td></td>
</tr>
<tr>
<td>Commit</td>
<td>EX4 adder</td>
<td>EX4 adder</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Writeback</td>
<td>EX5</td>
<td>EX5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**SweRV EL2 Core**

- **EL2 Core Complex**
  - **EL2 Core**
    - Fetch
    - Decode / Execute
    - Multiply Pipe
    - Divide
      - 34 cycle, out-of-
        pipe
    - Retire
    - Commit
  - **DCCM**
  - **ICCM**
  - **Icache**
  - **PIC**
  - **Debug**
  - **LSU Bus Master**
    - 64 bit AXI
  - **IFU Bus Master**
    - 64 bit AXI
  - **Debug Bus Master**
    - 64 bit AXI
  - **DMA Slave Port**
    - 64 bit AXI

- **EL2**
  - 2\textsuperscript{nd} generation design based on EH1
  - RV32IMC+Zbb+Zbs
  - 4 stage pipe to commit
  - Non-blocking microarchitecture

- **Zero cycle branch target buffer**

- **Worst case branch mispredict penalty of 1 cycle**
  - Close to 1 IPC on wide range of workloads

- **Fast Interrupt support**
  - Redirect directly to interrupt service routine upon interrupt

- **Enhanced DMA support**
  - Fully pipelined

- **Dhrystone of 2.0**

- **Coremark/MHz of 3.6**

- **Target frequency of 600 MHz**
  - 16 nm, worst case corner
SweRV EH2 core

- **EH2**
  - 2\textsuperscript{nd} generation design based on EH1
  - RV32IMAC+Zbb+Zbs
  - 8 stage pipe to commit
  - Non-blocking microarchitecture

- **Multithread support**
  - Up to 2 threads
  - Typical throughput gains of 1.6 to 2X
  - When ST IPC is 1.0 or less

- **Fast Interrupt support**
  - Redirect directly to interrupt service routine upon interrupt

- **Enhanced DMA support**
  - Fully pipelined

- **Dhrystone of 2.9**
- **Coremark/MHz**
  - 4.9 for 1 thread
  - 6.3 for 2 threads

- **Target frequency of 1.2 GHz**
  - 16 nm, worst case corner
SweRV EH2 pipeline

- **Fetch Address (FA)**
  - Each thread has a dedicated fetch address register
  - An LRU arbiter selects up to 1 thread to fetch each cycle

- **Fetch Buffers (FB)**
  - Each thread has 4 fetch buffers
    - 8B wide
    - Holds instructions from ICCM or I$
  - Dedicated aligner per thread

- **Instruction Buffers (IB)**
  - Each thread has 4 instruction buffers
  - Each cycle up to 2 threads are picked each cycle for decode
    - Typically one instruction from each thread is chosen if both threads are ready
    - Arbiter attempts to schedule the threads optimally

- **Integer Register File (IRF)**
  - Each thread has 31 integer registers

### Diagram Details
- **Fetch Address (FA)**
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SweRV EH2 pipeline: SMT example

- Thread arbitration done at
  - Fetch
  - Decode

- Above aligner
  - Threading is “vertical”
    - Only 1 thread per pipe state

- Aligner and below
  - Threading is “simultaneous”
    - Multiple threads per pipeline stage

- Commit stage
  - Commit up to 2 different threads per cycle
  - Commit groups == decode groups
EH2 msort example

- Homogeneous
  - Msort running on both threads
- Thread colors
  - Thread 0
  - Thread 1
- Measured at Commit Stage
  - Commit up to 2 instructions per cycle
- IPC of .79 for single thread:
  - Load-to-use of 11 cycles from external bus
- IPC of 1.50 for multi-thread
  - Multithread speedup of 1.9X over single-thread on same workload
  - Load-to-use of 11 cycles from external bus
SweRV EL2 and EH2 Performance

• SweRV EL2 Performance
  – For applications that hit to I$/ICCM and DCCM
    • IPC will be close to 1.0
      – Coremark ~.95 IPC
      – Dhrystone ~.98 IPC
    • Microarchitecture designed for 1 IPC

• SweRV EH2 Performance
  – ST performance
    • Essentially same as EH1
    – MT performance
      • Measured on wide range of ~120 mixed and non-mixed workloads
      • For ST IPC < 1.0
        – Average speedup of 1.9X
Flash Controller Applications

- SweRV RISC-V customized cores are finding new applications in flash controllers:
  - Main CPU processing host attachment I/F
  - Datapath CPU
  - Finite State Machine sequencers controlling individual NAND channels
  - Power management
  - Root of trust and encryption management
Conclusions

• Western Digital continues its commitment to RISC-V:
  – Continuing plans to deliver 1 billion cores through application in storage controllers

• Western Digital is releasing the 2nd generation of SweRV cores:
  – Powerful dual-threaded, dual-issue SweRV EH2
  – Ultrasmall low-power SweRV EL2

• RTL of the cores will be shared with the open source community via CHIPS Alliance:
  – https://github.com/chipsalliance/Cores-SweRV