Introducing Codasip SSP

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Who is Codasip?

- The **leading provider** of RISC-V processor IP
- Company founded in 2014 in the Czech Republic
  - Based on 10 years of university research on processor design automation
- Founding member of the RISC-V Foundation, www.riscv.org
- Now **Codasip GmbH**
  - Headquarters in Munich, Germany
  - R&D in Brno, Czech Republic
  - Offices in Silicon Valley, US, and Shanghai, Pudong PRC

Codasip Solutions

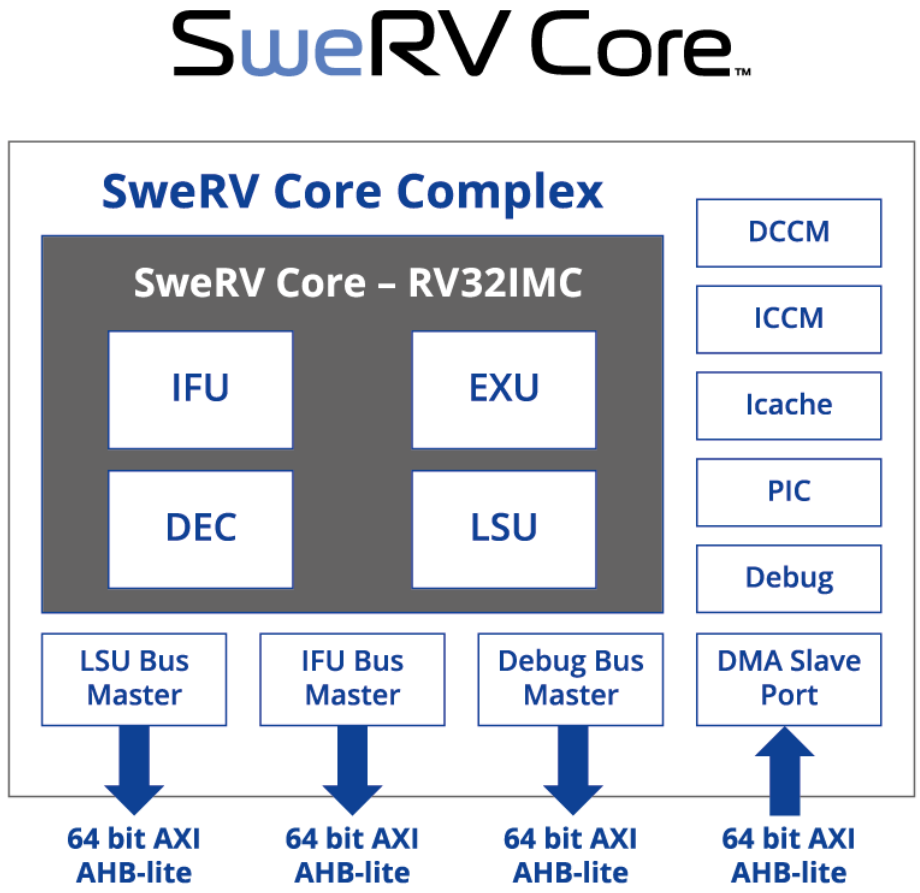
- **Codasip Bk =** portfolio of RISC-V processors
- **Codasip Studio** = unique design automation toolset for easy processor modification
  - Performance/power efficiency and low-cost
  - Algorithm acceleration (DSP, security, audio, video, etc.)
  - Profiling tools of embedded SW for tailoring processor IP
- **CodAL** = Codasip's own proprietary C-like language for processor architecture description

SweRV Support Package

New Product by Codasip

What is SweRV?

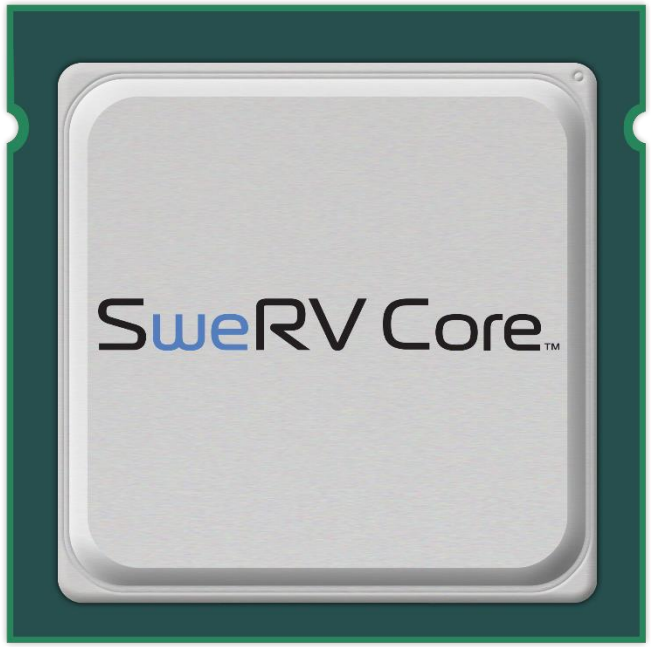
The first RISC-V-based open core developed by Western Digital



What is SSP?

SweRV Support Package

- First SSP available in **Q1 2020**
- Flexible engagement models



- Contains everything needed to deploy a SweRV core
  - Useful tools
  - Sample deliverables
  - Technical support

www.codasip.com/swerv

Why do I need the SSP?

- ✓ Provides **implementation files tied to 3rd party tools** that cannot be open-sourced:
  - Verification testbenches
  - Synthesis scripts
  - Integration into virtual platforms
- ✓ Includes access to **professional technical support**

Integrate the SweRV core with confidence while avoiding expensive license fees and royalties!

SSP Contents: Hardware

The latest SweRV core RTL

Implementation support

- Synthesis scripts for Design Compiler and Genus
- Simulation scripts for VCS, Questa, and Incisive

FPGA bitstream

- FPGA target and dev board including sample subsystem
- Support for JTAG debug
- Example software

Benchmark data and documentation

SSP Contents: Verification

Verification report with coverage data

Reference testbench

- System Verilog assertion monitors
- Verification IP

SSP Contents: Software

gcc compiler toolchain

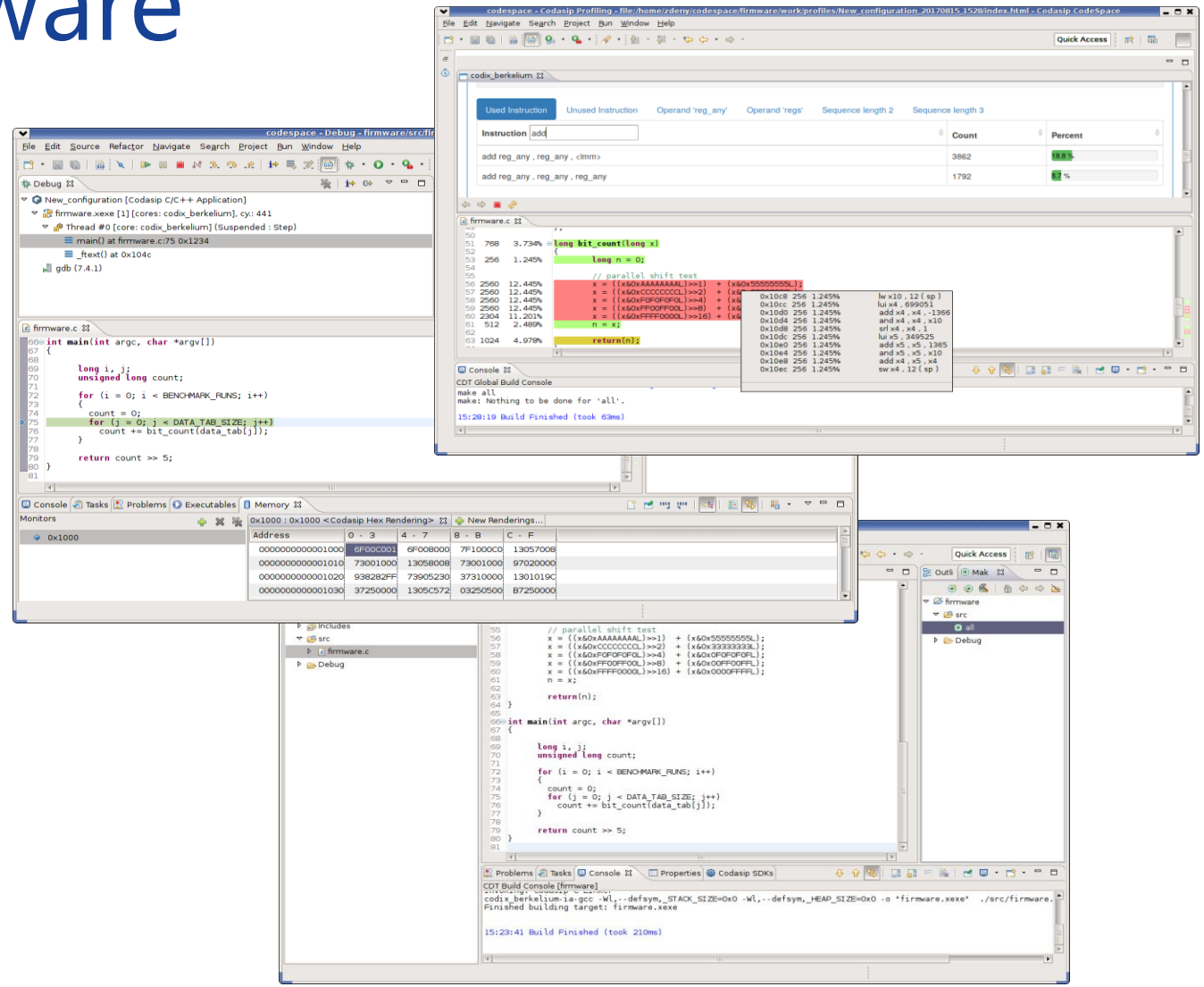
- Newlib
- Binutils
- Gdb

Eclipse IDE

- Graphical debug
- Profiler

Abstraction Layer

- Reset and initialization code
- OpenOCD for JTAG connectivity



Thank you!

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