SHAKTI Processor Project

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Processor IPs

- E-class 3-stage
- C-class 5-stage
- I-class* 12-stage

Bluespec System Verilog (BSV)

* Work in progress
E-Class

Features:
- 3-stage in-order
- ISA: RV[32/64] I [ACM]
- Can boot FreeRTOS, Zephyr

<table>
<thead>
<tr>
<th></th>
<th>Artix-7 FPGA</th>
<th>180nm ASIC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Config</strong></td>
<td>RV32IACM</td>
<td>RV64IACM</td>
</tr>
<tr>
<td><strong>LUTs</strong></td>
<td>2.5K</td>
<td>3K</td>
</tr>
<tr>
<td><strong>Clock freq.</strong></td>
<td>100 MHz</td>
<td>100 MHz</td>
</tr>
</tbody>
</table>

Src: [https://gitlab.com/shaktiproject/cores/e-class](https://gitlab.com/shaktiproject/cores/e-class)
**Processor IPs**

**Features:**
- 5-stage in-order
- ISA: RV[32/64] I [ACFDMNSU]
- Branch predictor + RAS
- Daisy-chained CSRs
- 1.72 DMIPS/MHz
- Can boot Linux kernel

**C-Class**

**Prototypes**
- 180nm
- 22nm (LP)

**Src:** [https://gitlab.com/shaktiproject/cores/c-class](https://gitlab.com/shaktiproject/cores/c-class)

<table>
<thead>
<tr>
<th>Artix-7 FPGA</th>
<th>65nm ASIC (LP)</th>
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<tbody>
<tr>
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<tr>
<td><strong>LUTs</strong></td>
<td><strong>Instances</strong></td>
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<td>RV32IACMNSU</td>
<td>RV32IACMNSU</td>
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<tr>
<td>4.5K</td>
<td>40.2K</td>
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<td>RV64IACMNSU</td>
<td>RV64IACMNSU</td>
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<tr>
<td>6.5K</td>
<td>80K</td>
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<tr>
<td><strong>Clock freq.</strong></td>
<td><strong>Clock freq.</strong></td>
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<tr>
<td>100 MHz</td>
<td>400 MHz</td>
</tr>
<tr>
<td>80 MHz</td>
<td>340 MHz</td>
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Core Configuration

**ISA**
RV[32/64][ACFDM], Supervisor and User support, User-trap support

**Branch Predictors**
History Size, BHT and BTB Sizes, RAS Size

**Caches**
Sets, Ways, Banks, Fill buffer size, ECC, TIMs

**MMU support**
Supervisor mode support, TLB Sizes, ASID width

**Misc**
PMP Size, Triggers, Debug support, Performance counters

**Simulation**
Verilator/VCS/Incisive, Coverage and Trace, Multi-threaded
Multicore

- Parameterizable no. of application cores (1-32 cores)
- Directory-based MSI cache coherence
- System management with monitor core
- TileLink-C bus protocol
- NoC with mesh topology

Safety critical applications

- Criticality aware NoC
- Triple Lock-Step (TLS) pipeline for fault tolerance*

* Work in progress

In Collaboration with Thales

SafeRV
Uncore IPs

- **Bus protocols**
  - AXI4/AXI4-Lite
  - TileLink-U/H

- **Bridges to/from AXI4 and AXI4-Lite with different data bus widths and clocks**

- **Posit-arithmetic Units + Compiler**

- **Peripherals**
  - SPI
  - PWM
    - Quad SPI
    - I2C
  - I2C
  - Watchdog
  - DMA
  - UART
  - PLIC

* For select FPGAs
**Offerings**

**Core + Uncore IP**
- Various classes of processors
- Bus protocols
- Peripherals
- Fully automated FPGA
- Bitstream generation

**Verification**
- CoCoTb VIPs: Coroutine Co-simulation Verification IPs*
- AAPG: Automatic Assembly Program Generator
- RiTA: RISC-V Trace Analyzer
- RISCV-Config Legalizer
- RISCOF: Compliance Testing
- RiVer: RISC-V Verification as a plugin infrastructure*

**Software**
- Integrated Development Environment (IDE)
- Software Development Kit (SDK)
- RISC-V OCaml and Mirage OS*

**Research***
- Systolic Array
- Crypto accelerators
- Side-channel attack resistance
- Fat-pointers
- Compartmentalization

* Work in progress
Start using Shakti today!

https://shakti.org.in