Syntacore™
Custom cores and tools

RISC-V compatible processor IP by Syntacore

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RISC-V Summit 2019

Syntacore introduction

IP company, founding member of RISC-V foundation

- Est 2015 , 40+ EEs
- HQ at Cyprus (EU), R&D offices in St. Petersburg and Moscow (Russia)

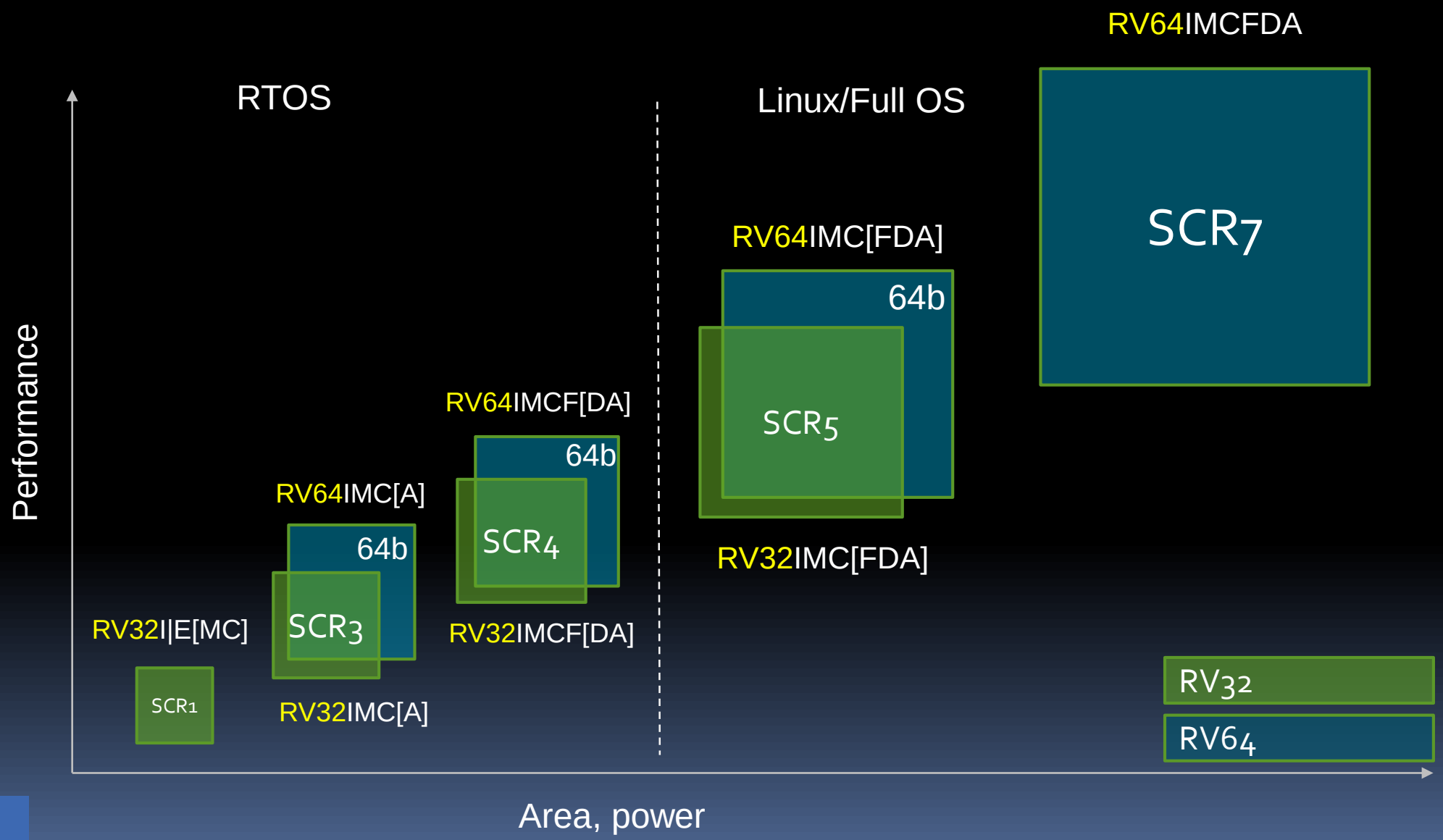
Develops and licenses state-of-the-art RISC-V cores

- Silicon-proven and shipping by customers
- 4+ years of *focused* RISC-V development
- Core team comes from 10+ years of highly-relevant background
- SDKs, samples in silicon, specs, full collateral

Full service to specialize CPU IP for customer needs

- One-stop workload-specific customization for 10X improvements
  - with tools/compiler support
- IP hardening at the required library node
- SoC integration and SW migration support

SCRx baseline cores



State-of-the art RISC-V CPU IP features

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Features			RTOS/ Bare Metal			Linux/ "Full" OS	
			SCR1* (FREE!)	SCR3	SCR4	SCR5	SCR7
Width		32bit	●	●	●	●	
		64bit		●	●	●	●
ISA			RV32I|E[MC]	RV[32|64]IMC[A]	RV[32|64]IMCF[AD]	RV[32|64]IMC[AFD]	RV64IMCAFD
Pipeline type			In-order	In-order	In-order	In-order	Superscalar
Pipeline, stages			2-4	3-5	3-5	7-9	10-12
Branch prediction				Static BP, RAS	Static BP, RAS	Static BP, BTB, BHT, RAS	Dynamic BP, BTB, BHT, RAS
Execution priority levels			Machine	User, Machine	User, Machine	User, Supervisor, Machine	User, Supervisor, Machine
Extensibility/customization			●	●	●	●	●
Execution units	MUL/DIV	area-opt	●	○	○		
		hi-perf	○	●	●	●	●
	FPU				●	●	●
Memory subsystem	TCM [w/ECC|parity]		○	○	○	○	○
	L1$ [w/ECC|parity]			○	○	●	●
	L2$ [w/ECC]					○	○
	MPU			●	●	●	●
	MMU, virtual memory					●	●
Debug	Integrated JTAG debug		●	●	●	●	●
	HW BP		1-2	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl
	Performance counters		○	○	○	○	○
Interrupt Controller	IRQs		8-32	8-1024	8-1024	8-1024	8-1024
	Features		basic	advanced	advanced	advanced+	advanced+
SMP support				up to 4 cores with coherency			up to 8-16 cores
I/F options	AHB		●	○	○	○	
	AXI4		○	●	●	●	●
	ACE						○

* Download SCR1 free at www.github.com/syntacore/scr1

Baseline cores:

- Clean-slate designs in System Verilog
- Configurable and extensible
- 100% compatible with major EDA flows

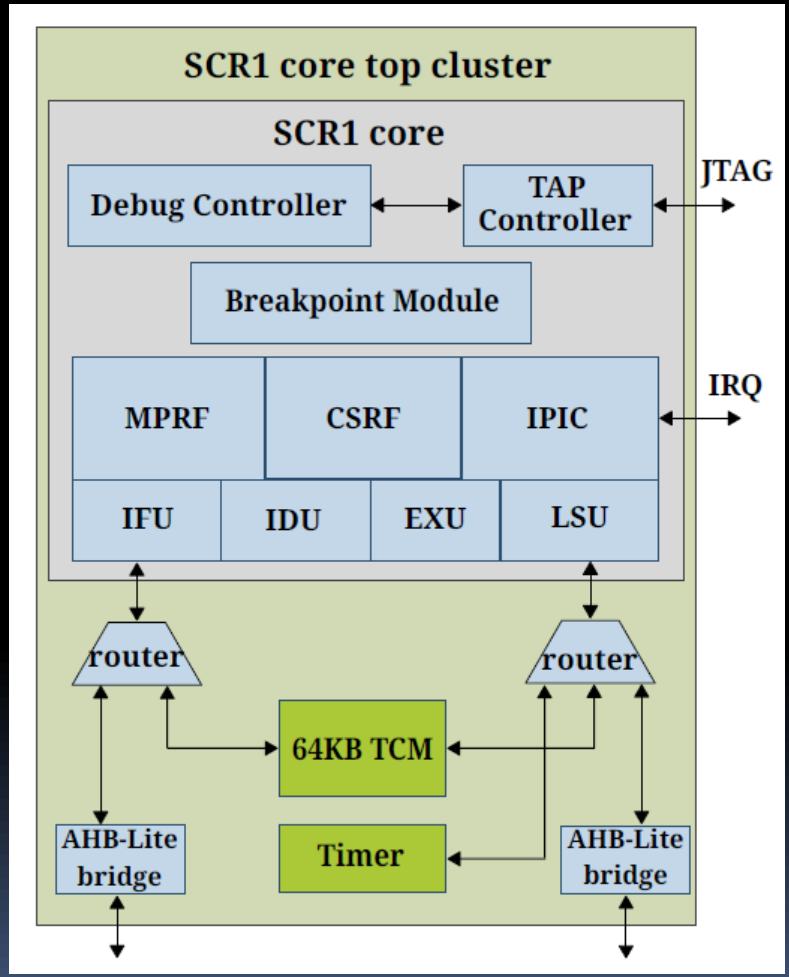
SCR1 overview

Industry-grade compact MCU core for deeply embedded applications and accelerator control

Open

- RV32I|E[MC] ISA
- 2 to 4 stages pipeline
- M-mode only
- Optional configurable IPIC
- Optional integrated Debug Controller
- Choices of the optional MUL/DIV unit
- Open sourced under SHL (Apache 2.0 derivative) since 2017
  - Unrestricted commercial use allowed

- High quality, silicon-proven free MCU IP
- In the top System Verilog Github repos in the world
  - https://github.com/syntacore/scr1
- Full collateral – TB & verification suite, SDK, specs, SW…
- Best-effort support provided, commercial offered



RV64 SCR7

Efficient mid-range application core

- RV64GC ISA
- SMP up to 8, later 16 cores
- Flexible uarch template, 10-12 stage pipeline
- Initial SCR7 configuration:
  - Decode and dispatch up to two instructions per cycle
  - Out-of-order issue of up to four micro-ops
  - Out-of-order completion, in-order retirement
- M-, S- and U-modes
- Virtual memory support, full MMU
- 16-64KB L1, up to 2MB L2 cache with ECC
- 1.2GHz+ @28nm
- Advanced debug with JTAG i/f

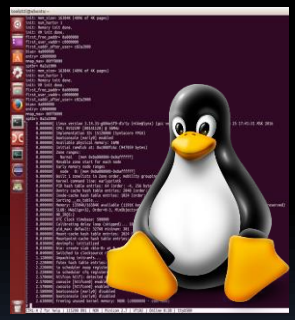
Demo

Flexible SCR7 uarch template

2-way SCR7 implementation

4-way SCR7 derivative

App-specific mix of Integer, FPU and LSU pipelines



Performance*, per MHz	DMIPS	-O2	3.25
		-best**	3.80
	Coremark	-best**	5.12

* Preliminary data, 2-way implementation, Dhrystone 2.1, Coremark 1.0, GCC 8.1 BM
** O3-funroll-loops -fpeel-loops -fgcse-sm -fgcse-las -flto

Fully featured SW development suite

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Stable IDE in production:

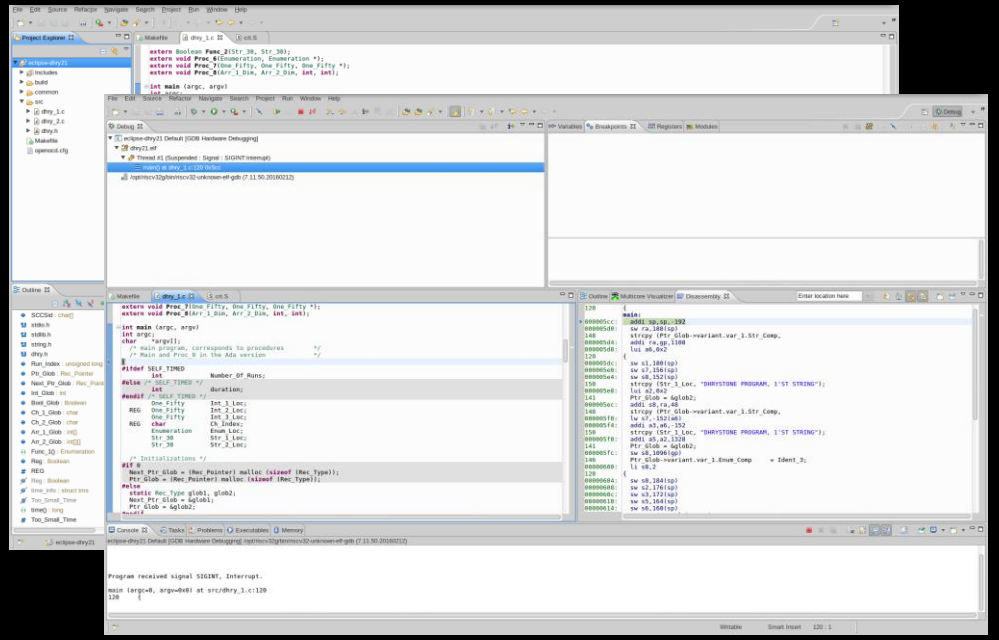
- GCC 8.1
- GNU Binutils 2.31.0
- Newlib 3.0
- GNU GDB 8.0.50
- Open On-Chip Debugger 0.10.0
- Eclipse 4.9.0

Hosts: Linux, Windows

Targets: BM, Linux (beta)

Also available:

- LLVM 5.0
- CompCert 3.1
- 3rd party vendors



Simulators:

- Qemu
- Spike
- 3rd party vendors

JTAG-based debug solutions:

Supports: Segger J-link, Olimex ARM-USB-OCD family, Digilink JTAG-HS2, more vendors soon

Number of commercial tools support SCRx cores

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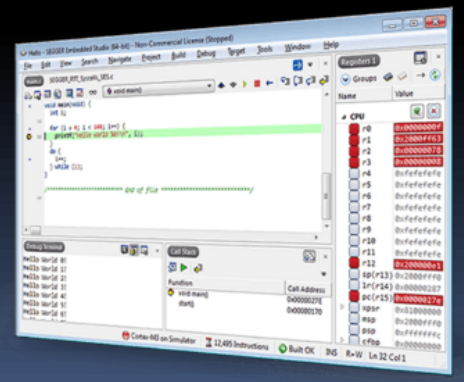
- Lauterbach Trace32

https://www.lauterbach.com/frames.html?pro/pro__syntacore.html

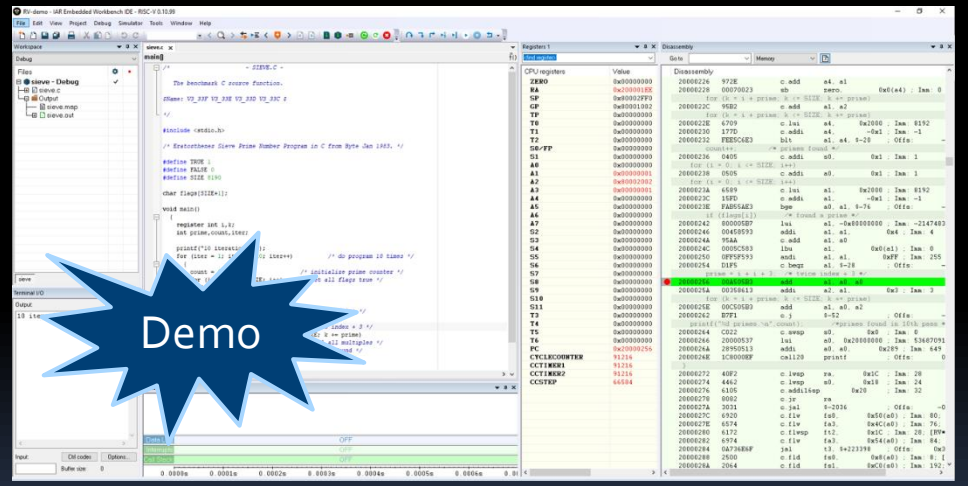
- Segger Embedded Studio

https://wiki.segger.com/Syntacore_SCR1_SDK_Arty



- IAR Embedded Workbench
- NEW!

https://www.iar.com/iar-embedded-workbench/#!?architecture=RISC-V



…more in 2020

Summary

- Syntacore offers high-quality RISC-V compatible CPU IP
  - Founding member, fully focused on RISC-V since 2015
  - Silicon-proven and shipping in mass-production
  - Turnkey IP customization services
    - with full tools/compiler support