RISC-V compatible processor IP by Syntacore

Alexander Redkin
Executive director

RISC-V Summit 2019
Syntacore introduction

IP company, founding member of RISC-V foundation
- Est 2015, 40+ EEs
- HQ at Cyprus (EU), R&D offices in St. Petersburg and Moscow (Russia)

Develops and licenses state-of-the-art RISC-V cores
- Silicon-proven and shipping by customers
- 4+ years of focused RISC-V development
- Core team comes from 10+ years of highly-relevant background
- SDKs, samples in silicon, specs, full collateral

Full service to specialize CPU IP for customer needs
- One-stop workload-specific customization for 10x improvements
  - with tools/compiler support
- IP hardening at the required library node
- SoC integration and SW migration support
## State-of-the-art RISC-V CPU IP features

<table>
<thead>
<tr>
<th>Features</th>
<th>SCR1+</th>
<th>SCR3</th>
<th>SCR4</th>
<th>SCR5</th>
<th>SCR7</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Width</strong></td>
<td>32bit</td>
<td>64bit</td>
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<tr>
<td><strong>ISA</strong></td>
<td>RV32I</td>
<td>RV32I</td>
<td>RV32I</td>
<td>RV32I</td>
<td>RV64I</td>
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<tr>
<td><strong>Pipeline type</strong></td>
<td>In-order</td>
<td>In-order</td>
<td>In-order</td>
<td>In-order</td>
<td>Superscalar</td>
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<tr>
<td><strong>Pipeline stages</strong></td>
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<td>3-5</td>
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<td>7-9</td>
<td>10-12</td>
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<tr>
<td><strong>Branch prediction</strong></td>
<td>Static BP, RAS</td>
<td>Static BP, RAS</td>
<td>Static BP, RAS</td>
<td>Dynamic BP, BTB, BH-T, RAS</td>
<td>Dynamic BP, BTB, BH-T, RAS</td>
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<tr>
<td><strong>Execution priority levels</strong></td>
<td>Machine</td>
<td>User, Machine</td>
<td>User, Machine</td>
<td>User, Supervisor, Machine</td>
<td>User, Supervisor, Machine</td>
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<tr>
<td><strong>Extensibility/customization</strong></td>
<td>●</td>
<td>●</td>
<td>●</td>
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<tr>
<td><strong>Execution units</strong></td>
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<tr>
<td>MUL/Div</td>
<td>area-opt</td>
<td>●</td>
<td>●</td>
<td>●</td>
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<tr>
<td>FPU</td>
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<tr>
<td>Memory subsystem</td>
<td>TCM [w/ECC</td>
<td>parity]</td>
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<tr>
<td>L1S [w/ECC</td>
<td>parity]</td>
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<td>L2$ [w/ECC]</td>
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<td>MPU</td>
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<tr>
<td>MMU, virtual memory</td>
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<td>Debug</td>
<td>Integrated TAG debug</td>
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<td>1-8 adv ctrl</td>
<td>1-8 adv ctrl</td>
<td>1-8 adv ctrl</td>
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<td>HW BP</td>
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<td>8-1024</td>
<td>8-1024</td>
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<tr>
<td>Features</td>
<td>basic</td>
<td>advanced</td>
<td>advanced</td>
<td>advanced+</td>
<td>advanced+</td>
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<tr>
<td>SMP support</td>
<td>up to 4 cores with coherency</td>
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<td>up to 8-16 cores</td>
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<tr>
<td>I/F options</td>
<td>AH-B</td>
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<td>AXI4</td>
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<td>ACE</td>
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**Baseline cores:**
- Clean-slate designs in System Verilog
- Configurable and extensible
- 100% compatible with major EDA flows
SCR1 overview

Industry-grade compact MCU core for deeply embedded applications and accelerator control
- RV32|E[MC] ISA
- 2 to 4 stages pipeline
- M-mode only
- Optional configurable IPIC
- Optional integrated Debug Controller
- Choices of the optional MUL/DIV unit
- Open sourced under SHL (Apache 2.0 derivative) since 2017
  - Unrestricted commercial use allowed

- High quality, silicon-proven free MCU IP
- In the top System Verilog Github repos in the world
  - https://github.com/syntacore/scr1
- Full collateral – TB & verification suite, SDK, specs, SW...
- Best-effort support provided, commercial offered
**RV64 SCR7**

Efficient mid-range application core

- RV64GC ISA
- SMP up to 8, later 16 cores
- Flexible uarch template, 10-12 stage pipeline
- **Initial SCR7 configuration:**
  - Decode and dispatch up to two instructions per cycle
  - Out-of-order issue of up to four micro-ops
  - Out-of-order completion, in-order retirement
- M-, S- and U-modes
- Virtual memory support, full MMU
- 16-64KB L1, up to 2MB L2 cache with ECC
- 1.2GHz+ @28nm
- Advanced debug with JTAG i/f

**Performance**, per MHz

<table>
<thead>
<tr>
<th></th>
<th>DMIPS</th>
<th>Coremark</th>
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<tbody>
<tr>
<td><code>-O2</code> best**</td>
<td>3.25</td>
<td>3.80</td>
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<tr>
<td><code>-best**</code></td>
<td>5.12</td>
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</tbody>
</table>

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* Preliminary data, 2-way implementation, Dhrystone 2.1, Coremark 1.0, GCC 8.1 BM
** OS-funroll-loops -fpeel-loops -fgcse-sm -fgcse-las -flto
Fully featured SW development suite

Stable IDE in production:

- GCC 8.1
- GNU Binutils 2.31.0
- Newlib 3.0
- GNU GDB 8.0.50
- Open On-Chip Debugger 0.10.0
- Eclipse 4.9.0

Hosts: Linux, Windows
Targets: BM, Linux (beta)

Also available:

- LLVM 5.0
- CompCert 3.1
- 3rd party vendors

Simulators:

- Qemu
- Spike
- 3rd party vendors

JTAG-based debug solutions:
Supports: Segger J-link, Olimex ARM-USB-OCD family, Digilink JTAG-HS2, more vendors soon
Number of commercial tools support SCRx cores

- **Lauterbach Trace32**
  [Image](https://www.lauterbach.com/frames.html?pro/pro__syntacore.html)

- **Segger Embedded Studio**
  [Image](https://wiki.segger.com/Syntacore_SCR1_SDK_Arty)

- **IAR Embedded Workbench**
  [Image](https://www.iar.com/iar-embedded-workbench/#!?architecture=RISC-V)

- **NEW!**

...more in 2020
Summary

- Syntacore offers high-quality RISC-V compatible CPU IP
  - Founding member, fully focused on RISC-V since 2015
  - Silicon-proven and shipping in mass-production
  - Turnkey IP customization services
    - with full tools/compiler support