OpenHW Group
2020 BHAG
BIG HARRY AUDACIOUS GOAL

CORE-V™ Chassis

- production ready,
- CORE-V CV64A & CV32E cores,
- deep sub-micron SoC,
- on an eval board,
- running Linux / Zephyr
- Tapeout 2H, 2020
- Linux capable 1.5GHz CV64A host CPU and CV32E coprocessor
- X32/x16 (LP)DDR4, DDR3L memory
- 3D / 2D GPUs with OpenGL support
- MIPI-DSI / CSI display / camera controllers
- Security: DRM Ciphers, key storage, random number generator, etc.
- GigE MAC
- PCIe 2.0 x1 port
- 2 USB 2.0 interfaces
- 3 SDIO interfaces for boot source, storage, etc.

![Board Layout Diagram]
• CV64A application 64bit RV64GC processor core IP (Ariane core)
  • Linux Capable
    • Tightly integrated D$ & I$
    • M, S & U privilege modes
    • TLB, SV39
    • Hardware PTW
  • Optimized for performance
    • Frequency: 1.5GHz
    • Area:~175kGE
    • Critical path: ~25 logic levels

• 6-stage pipeline
  • In-order issue
  • Out-of-order write-back
  • In-order commit
• CV32E embedded 32bit RV32IMFCXpulp processor core IP (RI5CY core)
  • 4-stage pipeline
  • 70K GF22 nand2 gate equivalents gate + 30KGE for FPU
  • Coremark/MHz 3.19
• Includes various extensions
  • pSIMD, Fixed point, Bit manipulations, HW loops
• Silicon Proven
  • SMIC130, UMC65, TSMC55LP, TSMC40LP, GF22FDX

• Floating Point Unit
  • Iterative DIV/SQRT (9 cycles)
  • Parametrizable latency for MUL, ADD, SUB, Cast
  • Single cycle load, store
CORE-V™ Chassis - Possible Processor Complex – CV64 + CV32 cluster

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CORE-V™ Chassis - Possible Processor Complex – CV64A + CV64V Vector Core
CORE-V Chassis – Call for Participation

• Join the OpenHW Group to drive the CORE-V Chassis project

  • CV64A and CV32 verification test bench

  • CV64A bus interfaces and cache coherency support

  • CV64A IPC improvements

  • CV64A and CV32E OS porting / development environment

  • ... and more ...