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# RISC-V: A Zero Trust Avionics Security Architecture (ASA)

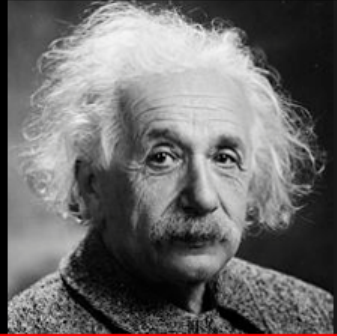
## End to End Flight Security

11 December, 2019

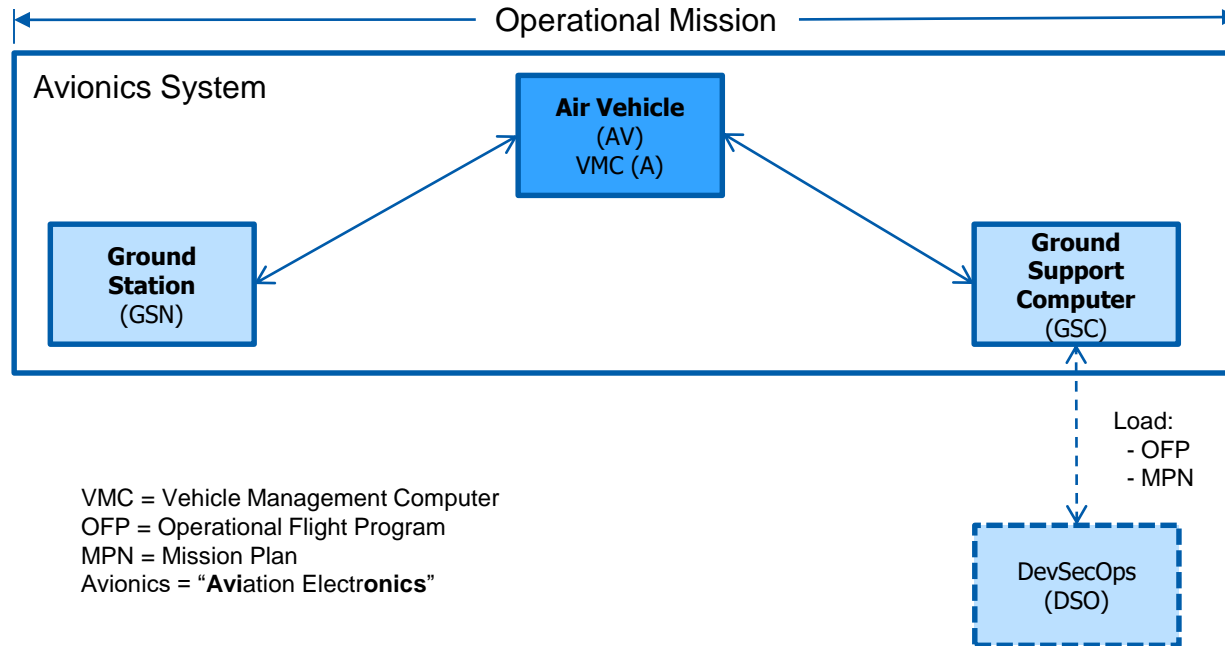
Kevin Kinsella  
Architect – Cyber Resilient Vehicle Management System

**If you can't explain  
it simply, you  
don't understand  
it well enough.**

Einstein



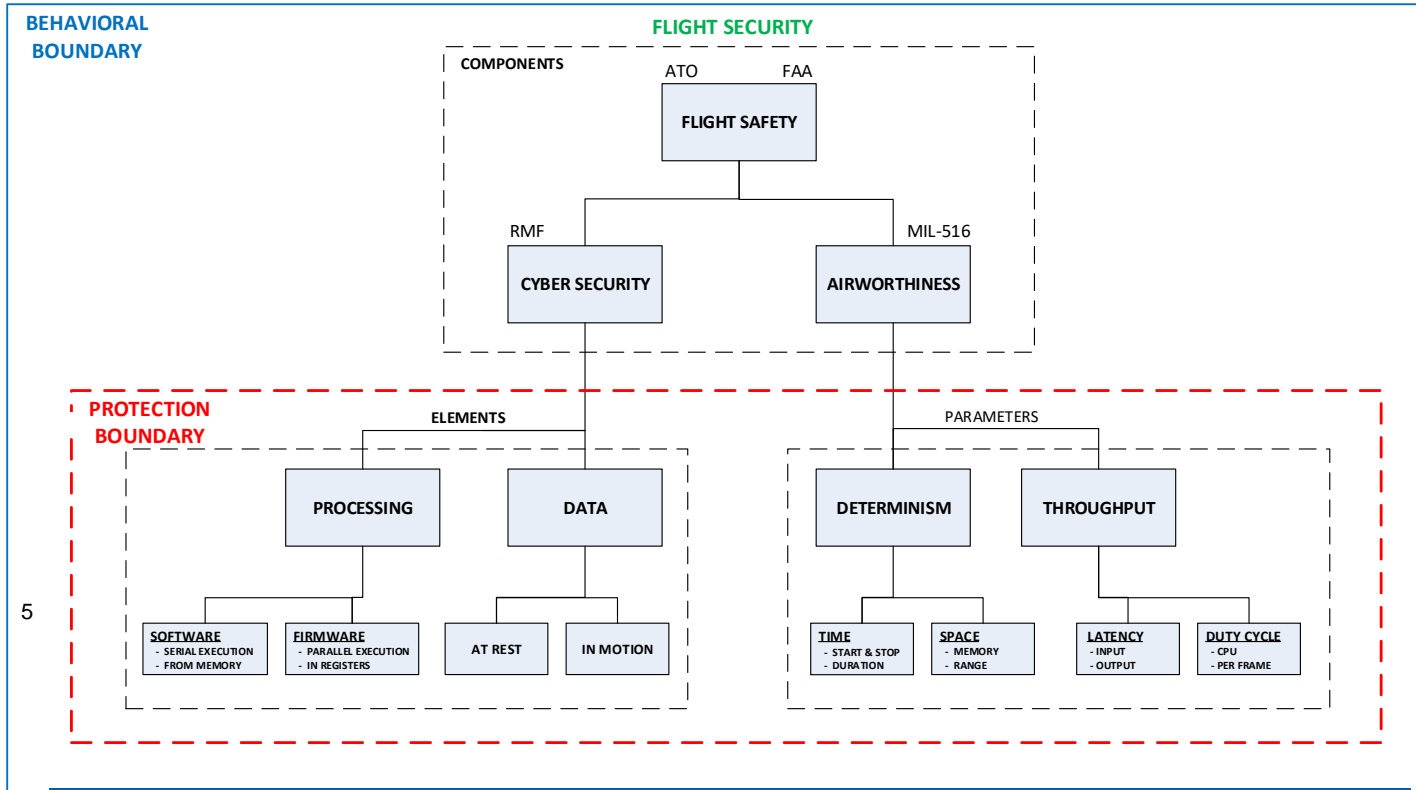
# Avionics Security Architecture (ASA)



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Top Level Requirement: The ASA *shall* provide Flight Security

# Requirement: Flight Security



**Flight Security / Flight Safety == two sides of the same coin**

# RISC-V for ASA: Why ?

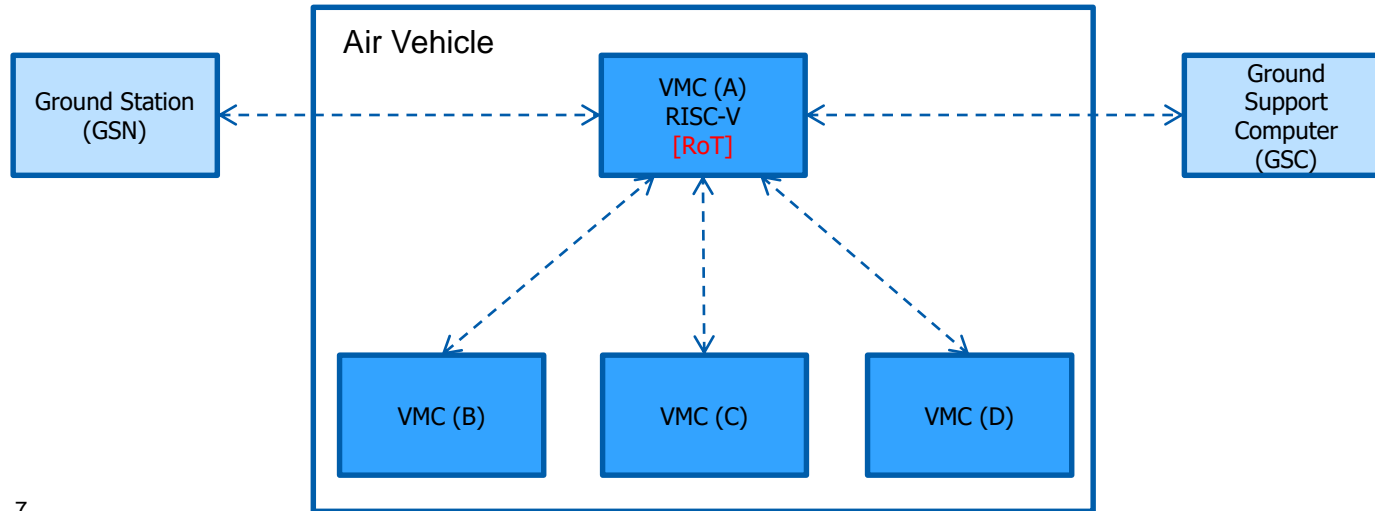
- RISC-V allows “Future Proof” VMC (Vehicle Management Computer) implementations:
  1. RISC-V is flexible
    - Processing can be instantiated in
      - » Hard core (in metal)
      - » Soft core (in fabric)
  2. RISC-V is adaptable
    - Soft cores can tailor security for each program
  3. RISC-V is customizable
    - ISA can be extended to support AI / ML / Neural Net monitoring

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RISC-V = “Future Proof” VMCs

# Flight Security Assumes “Zero Trust”

- The VMCs establish and extend the Root of Trust (RoT)

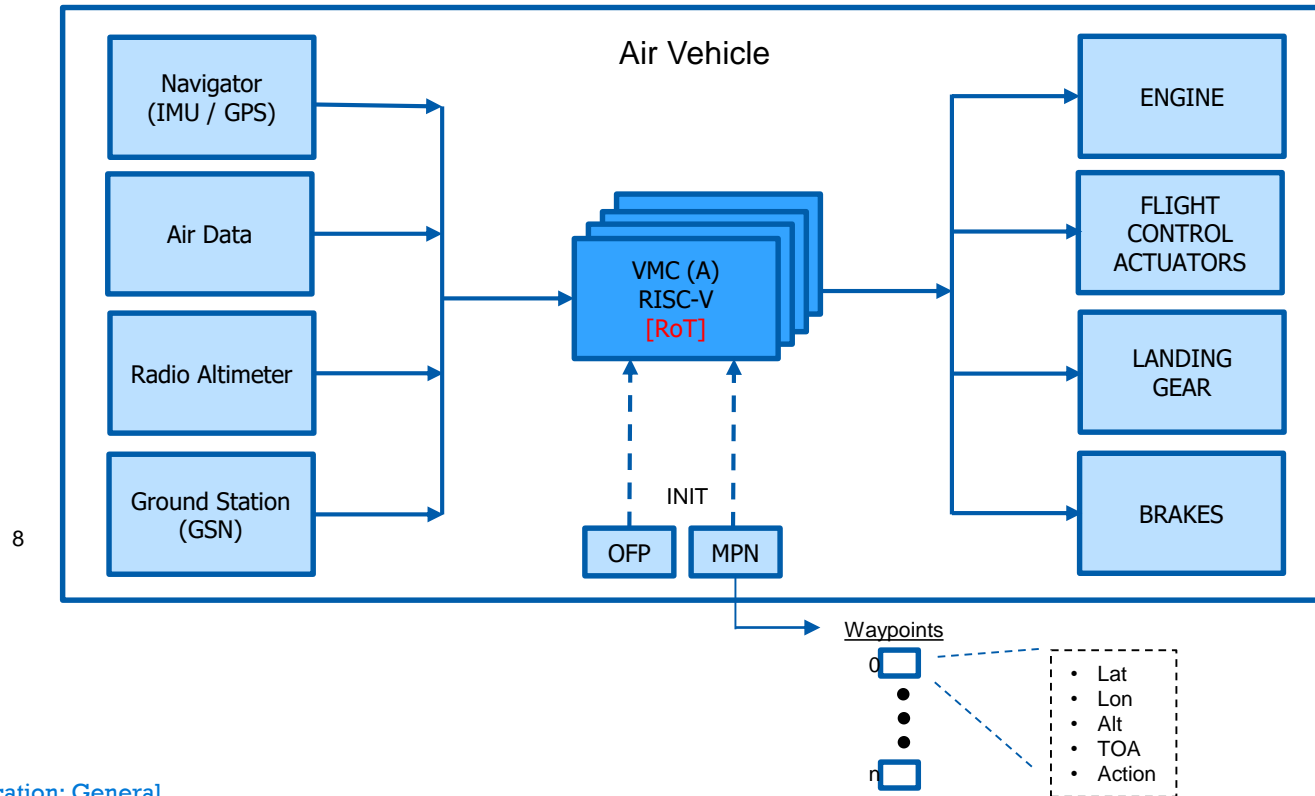


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- Trust is anchored in hardware FPGA PUF (Physically Unclonable Function)
- Trust is extended by confidentiality, integrity and authentication
- Cyber resiliency is created by monitoring and recovering

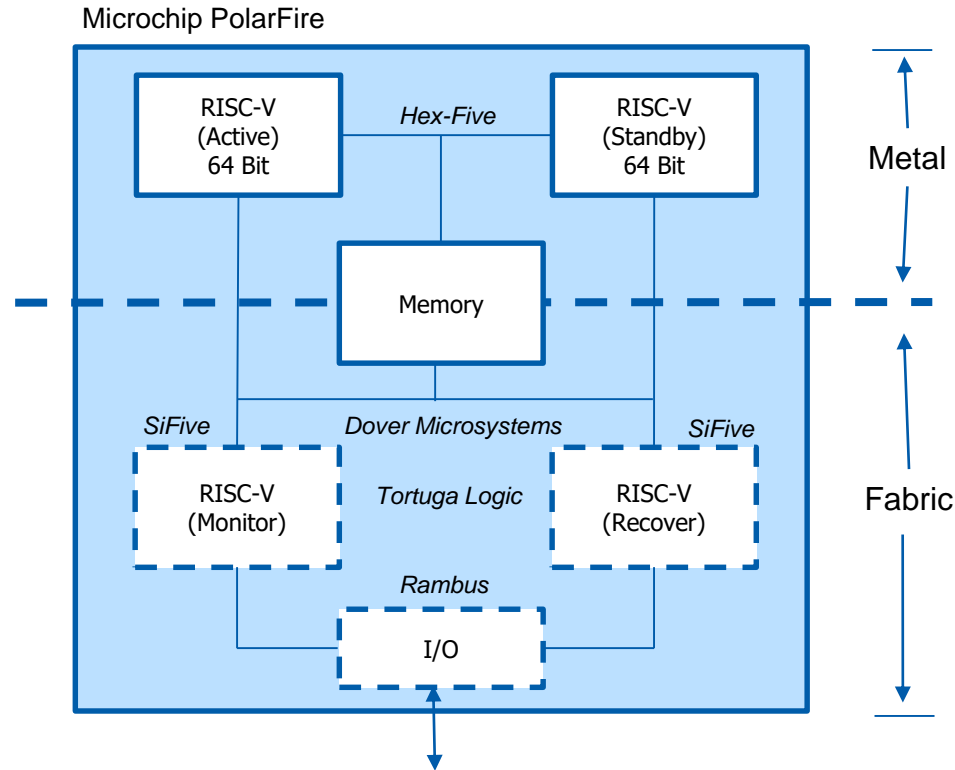
# VMCs Implement Cyber Resiliency

- The VMCs monitor and respond to cyber events to safely fly the air vehicle





# RISC-V: How? Leverage Mature Ecosystem



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Hard/soft CPUs, RoT, multi-zone, isolation, execution security

# RISC-V for ASA: When?

- After the New Year, just Look Up ... 😊

**RISC-V will be flying in an operational satellite system!**

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