Debugging Heterogeneous SoCs Containing a Mix of RISC-V and non-RISC-V Cores

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System-on-Chip (SoC) Design Trends

• SoC design is becoming more complex as chip designers pack more and more features on to a single device to meet market demands.

• To meet feature, power consumption and performance requirements, designers are utilizing multi-core designs and integrating processor architectures from different companies (i.e. heterogeneous cores) onto a single SoC.

• It is now becoming common to find SoCs with multiple disparate cores from vendors such as ARM, ARC (Synopsys), MIPS (Wave Computing) and RISC-V.
The following example multi-core heterogeneous SoC has three ARM and two RISC-V cores:

- DAP supports CoreSight debug access via Advanced Peripheral Bus (APB).
- DAP supports System access via Advanced High-performance Bus (AHB) (not shown)
Too Many Tools!

• In Multi-core designs each core typically currently comes with its own toolset which only supports the specific vendor’s core. This is problematic as:
  • Engineers must currently use separate toolsets for each core in their SoC
  • SoC-wide debug and verification is not possible as toolsets can only work with a specific core
  • Multi-core, heterogeneous support within a single toolchain is currently not possible!
Ashling RiscFree™ Overview

- Eclipse based Integrated Development Environment (IDE) for RISC-V development
- Seamless environment for multi-core heterogeneous software development including support for writing, building, simulating and hardware debugging
- Multi-core heterogeneous Debugger with Ashling Opella-XD probe support
RiscFree™ Heterogeneous Multi-core Debug Support

- A single Opella-XD debug probe using a single debug interface (JTAG, cJTAG or SWD) can debug all “connected” cores
- Currently supports multi-core debug support using RISC-V, ARM and Synopsys ARC cores
RiscFree™ Debug Launch Settings

Create, manage, and run configurations
RiscFree™ Debug View Showing Multiple Launches
RiscFree™ Multiple Core Specific Views (e.g. Registers)
Conclusion

• Heterogeneous multi-core SoC designs utilizing RISC-V and other vendor cores (e.g. ARC, ARM, DSPs, MIPS) are becoming more common

  • Using core vendors toolsets is problematic as separate toolsets are needed for each core in the SoC
  • SoC-wide debug and verification is not possible as existing core vendor toolsets only work with their specific core

  • RiscFree™ provides an integrated multi-core, heterogeneous based solution within a single toolchain

• Please drop by to see Ashling at booth #216 later to find out more

• Feel free to contact me with any follow-up questions or feedback.

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  More info: https://www.ashling.com/multi-core/