Andes RISC-V Processor Solutions
From MCU to Datacenters

Charlie Su, Ph.D.
CTO and EVP

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Agenda

- Andes Overview
- Andes 27-Series Cores and Vector Processing Unit
- Andes Superscalar 45-Series Cores
- Summary
<table>
<thead>
<tr>
<th>Silicon Valley Tie</th>
<th>14-Year CPU IP Company</th>
<th>&gt;1 Bn Annual Run Rate of Andes-Embedded SoC</th>
<th>Founding Platinum Member and Major Contributor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>• Core R&amp;D from AMD, DEC, Intel, MIPS, nVidia, and Sun</td>
<td>• IPO in 2017; HQ in Taiwan</td>
<td>• ~200 customers in TW, CN, US, EU, JP, KR</td>
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<tr>
<td></td>
<td></td>
<td>• AndeStar™ V1-V3, V5 (RISC-V)</td>
<td>• Chairing Task Groups</td>
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<td>• Contributing to GNU, LLVM, uBoot, glibc, Linux, etc.</td>
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</table>
**Andes V5 Architecture**

- **V5: RISC-V + Andes Extensions**
- **V5 processors offer**
  - Higher per-MHz performance
  - Smaller code size with CoDense™
  - Rich features for embedded systems
    - Full cache management
    - StackSafe™
    - QuickNap™/PowerBrake
    - Misaligned loads/stores
  - Andes Custom Extensions™ (ACE) with powerful automation tool COPILOT
  - CAD tool friendly RTL in Verilog
  - Flexible configurations with GUI tool
V5 Adoptions: From MCU to Datacenters

- Edge to Cloud:
  - ADAS
  - AIoT
  - Blockchain
  - FPGA
  - MCU
  - Multimedia
  - Security
  - Wireless (BT/WiFi)

- Datacenter AI accelerators
- SSD: enterprise (& consumer)
- 5G macro/small cells

- ~50% with AI
- 40nm to 7nm
V5 Adoptions: Cores in SoC

- Single core
- 2-8 cores
- > 30 cores
- > 100 cores
- > 1000 cores

Taking RISC-V® Mainstream
# Andes V5 Processor Lineup

<table>
<thead>
<tr>
<th></th>
<th>RV32</th>
<th>RV64</th>
<th>Vector Ext.</th>
<th>Superscalar</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cache-Coherent 1-4 Cores</strong></td>
<td>A25MP</td>
<td>AX25MP</td>
<td><strong>27-Series:</strong> MemBoost Vector Ext.</td>
<td><strong>45-Series:</strong> MemBoost Dual Issue.</td>
</tr>
<tr>
<td><strong>Linux with FPU/DSP</strong></td>
<td>A25</td>
<td>AX25</td>
<td><strong>NX27V A27/AX27 and more.</strong></td>
<td><strong>N45/NX45 D45/DX45 A45/AX45 and more.</strong></td>
</tr>
<tr>
<td><strong>Fast/Compact with FPU/DSP</strong></td>
<td>N25F D25F</td>
<td>NX25F</td>
<td><strong>5-stage</strong> (1.1 GHz)</td>
<td><strong>5-stage</strong> (1.1 GHz)</td>
</tr>
<tr>
<td><strong>5-stage</strong> (1.1 GHz)</td>
<td><strong>8-stage</strong> (1.2 GHz)</td>
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</table>

Note: Common features are RV*IMACN, Caches, LM, ECC, BrPred, CoDense™, PowerBrake, StackSafe™ ACE (Andes Custom Extension™); Frequencies at 28nm

**Taking RISC-V® Mainstream**
AndesCore™ 27 Series

**A27/AX27 and NX27V**
- RV*GC-N-P
- 5-stage single-issue
- Leveraging the mature 25-series; so same scalar performance

**MemBoost**
- Skip unnecessary writes to dcache
- Multiple outstanding data accesses
- I/D cache prefetch
- Performance over 25-series:
  - 50% higher memory bandwidth
  - 50% memory latency
NX27V VPU Overview

- **VPU**: Vector Processing Unit
- **RVV spec**: ongoing 0.8
- **Data formats**:
  - SEW supported: int8, int16, int32, fp16, fp32
  - Extension formats: bfloat16 and int4
- **Support LMUL 1, 2, 4, 8**
- **VPU main configurations**:
  - SIMD width and VLEN (bits): 128, 256, and 512
- **Functional units chainable, with dedicated IQ, most fully pipelined**
- **Wide system bus for data accesses**
- **Vector Registers as operands for ACE instructions**
  - Usage example: custom vector load/store from a dedicated memory port

**Verification**: leverage/enhance Google UVM, working with Imperas
NX27V VPU: A Tight Loop

LMUL=8: 8 u-instructions are issued.

time

vf3 v0, v20, f0

vi1 v20, v10, t1

vf2 v20, v20

: 1 u-instruction in progress

: 8 u-instruction in sequence

: Chaining
NX27V: Development Tools

- Assembler/Debugger
- Compiler: intrinsic functions
- Neural Net Library for RVV (in addition to RVP)
- Near-cycle accurate performance simulator
- Pipeline/resource analyzer
- All integrated in AndeSight IDE
## AndesCore™ 45 Series

### Full RISC-V ISA:
- N45/NX45: RV*GCN
- D45/DX45: RV*GCN+ P
- A45/AX45: RV*GCN+ P + MMU
- More later

### Common features:
- Eight-stage dual-issue pipeline
- Late ALUs enables 0-cycle load-use penalty and dual issue of dependent instructions
- Low-power branch prediction scheme
- MemBoost memory subsystem

<table>
<thead>
<tr>
<th></th>
<th>F1</th>
<th>F2</th>
<th>ID</th>
<th>II</th>
<th>EX</th>
<th>MM</th>
<th>LX</th>
<th>WB</th>
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<tbody>
<tr>
<td>ALU</td>
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<td>I$</td>
<td>ILM</td>
<td>DEC</td>
<td>ISS</td>
<td>AG</td>
<td>D$</td>
<td>DLM</td>
<td>Multiplier</td>
<td>DSP</td>
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<tr>
<td>Floating Point Unit</td>
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($/LM: 2^{nd} cycle for alignment)
## 45 Series: Performance

### Performance:
- Max. frequency @28HPC+ (worst case): > 1.2 GHz
- \(~50\%\) faster than 27/25-series at the same frequency

<table>
<thead>
<tr>
<th>Benchmark (/MHz)</th>
<th>N25</th>
<th>N45</th>
<th>Speedup</th>
<th>N25</th>
<th>N45</th>
<th>Speedup</th>
<th>N25</th>
<th>N45</th>
<th>Speedup</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coremark</td>
<td>3.58</td>
<td>5.40</td>
<td>1.51</td>
<td>3.53</td>
<td>5.38</td>
<td>1.52</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMIPS (no-inline)</td>
<td>1.97</td>
<td>2.89</td>
<td>1.48</td>
<td>2.13</td>
<td>3.14</td>
<td>1.47</td>
<td></td>
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</tr>
<tr>
<td>Embench-IOT (0.5)</td>
<td>1.82</td>
<td>2.68</td>
<td>1.47</td>
<td>1.91</td>
<td>2.77</td>
<td>1.45</td>
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</table>
■ LLVM:
  ● Good compiler infrastructure
  ● Good interface as a backend for “AI Compilers”

■ Andes is a major contributor to LLVM (and LLD maintainer)

■ V5 LLVM is
  ● 15%~25% faster than upstream LLVM (Embench and EEMBC)
  ● 25% smaller than upstream LLVM (Embench)
  ● As fast and small as V5 GCC (+/- 1%)

<table>
<thead>
<tr>
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<th>NX45</th>
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<tr>
<td>Embench-IOT</td>
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</tr>
<tr>
<td>Performance (/MHz)</td>
<td>2.68</td>
<td><strong>2.72</strong></td>
</tr>
<tr>
<td>Code Size (KB)</td>
<td>52</td>
<td><strong>52</strong></td>
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AndeSight™: Professional IDE

- Eclipse-based, enriched by 14-year effort

Taking RISC-V® Mainstream
Andes RISC-V Serving Emerging SoC from Edge to Cloud

Performance & Extensibility
- Leading PPA and code size
- Rich data processing in P, V, and ACE

Configurability
- Flexible configurations for rich features

Maturity
- Compiler optimizations, and SW stacks
- Comprehensive features in AndeSight IDE
Thank You!
Thank you