Where RISC-V Sees Strong Momentum
An Overview of Real-time, Performance Opportunity

Driving Innovations™
# 10+ Years Head Start in RISC-V Processor Solutions

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<table>
<thead>
<tr>
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<tbody>
<tr>
<td>200 commercial licensees</td>
<td>~ 100 design wins in RISC V</td>
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<tr>
<td></td>
<td>AI, AR/VR, FPGA, Consumer, Security</td>
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<td>200 people; 80% in R&amp;D</td>
<td>R&amp;D in Taiwan &amp; US FOCUSED on processors</td>
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<td>First to ship VPU in ‘19</td>
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<tr>
<td>Found in 2005; Public since 2017</td>
<td>8 RISC 32-/64-bit processors developed</td>
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<tr>
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<td>&gt;1B units/year shipped since 2018</td>
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<td>Complete ecosystem before RISC-V</td>
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<tr>
<td>Founding member and Major Contributor to RISC-V</td>
<td>Tool chain contribution (LLVM, GCC)</td>
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<td>ISA extensions (PLIC, SIMD)</td>
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Products Focused on Realtime Performance/Cost

- **RISC-V business started in:**
  - Cost reduction from ARM
  - FSM replacement in FinFET SOCs
- **RISC-V not ready for MCU & phone, tablet, yet**
- **Andes focuses on real-time & performance**
  - Bringing accelerators closer to CPUs
  - AI/AR/VR/CV/etc. in-between layer work-load
  - Efficiently move data
How to Combine Flexibility & Performance/Watt?
ACE ISA extension for programming/support of accelerator
Data permutation for re-ordering data
VPU for exceptional computation support
Use RISC-V to Coordinate with Accelerator

- Issue instructions as coprocessor
  - "fire & forget"; stall when busy

- Pulling for accelerator status
  - "wait for ready"

- "load/store" data
  - Load from SRAM to re-format or process (e.g. vector processor)
  - Store to SRAM after permutation
ACE and COPILOT Environment

Concise RTL
Verilog user.v
Script user.ace

Automated Env. For Cross Checking
Test Case Generator

Extended RTL
Extended ISS

Extended Tools
Extended ISS
Extended RTL

Compiler
Asm/Disasm
Debugger
CPU ISS
CPU RTL

Extensible Baseline Components

COPILOT™
Custom-OPtimized Instruction developent Tools
NX27-V100 First RISC-V Vector Engine Shipped in Industry!

- RVV v0.8 support*
- AI optimized: support for BFloat16 & INT4
- 1GHz, < 0.3mm² worst case in TSMC 7nm FF+
- Configurable & scalable
  - Vector length 128-bits to 1024-bits
  - Variety of ALUs
- Low power
  - Multi-level clock-gating
  - Units-off if not executing
- Simple to implement
  - In-order, 1R/W SRAM, cell based

<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
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<tbody>
<tr>
<td>3.6</td>
<td>vstart CSR is always 0</td>
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<tr>
<td>7.5</td>
<td>no Vector strided load/store</td>
</tr>
<tr>
<td>7.6</td>
<td>no Vector indexed load/store</td>
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<tr>
<td>7.7</td>
<td>no Unit-stride Fault-only-First load</td>
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<tr>
<td>7.8</td>
<td>no Zvisseg extension</td>
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<tr>
<td>8</td>
<td>no Zvamo extension</td>
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<tr>
<td>19</td>
<td>no Zvediv extension</td>
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<td>No 64-bit floating point ops</td>
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Permutation Optimization for Low Power Data Movement

Use RISC-V Vector Engine
MemBoost Enhances Memory Performance

Data Cache Write-Around

Read/Write allocates to cache line
The cache line is evicted later
Write-around reduces memory accesses

Instruction and Data Pre-fetch

Next instruction line fetch
Data streaming fetch

Multiple Requests Support Out-of-Order Completion

Expanded memory bandwidth

Supports Multiple Requests

Confidential
Real-Time, Performance Key to RISC-V Adoption

- RISC-V used to be low-cost
- RISC-V now has new purpose
  - Give designers ISA freedom
  - Much better vector/SIMD

CPU-Accelerator
Vector Processor
Memory Optimization