While RVTA gathers industry and academia expertise, momentum of RISC-V is building up primarily by business and research opportunities.

Highly Specialized Supply Chain
Foundry (Worldwide 70% market share) and OSAT worldwide 50% are both world leading, and IC design 20% next only to the U.S., with extensive IP and design services.
## Examples of RISC-V announcements

**RISC-V Taiwan Alliance (RVTA)**

<table>
<thead>
<tr>
<th>Foundry</th>
<th>IP</th>
<th>Design service</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td><strong>Andes</strong> Launches RISC-V FreeStart Program with its Commercial-Grade CPU N22.</td>
<td><strong>Faraday</strong> Unveils RISC-V ASIC Solution to Support Edge AI and IOT SoCs, proven in mass production.</td>
</tr>
</tbody>
</table>

### Highlight: Processing in Memory*

- **Powerchip** forms AI Memory Corp. for solutions to the memory wall in computing.
Unprecedented scalable ultra-efficient PIM* architecture and chip

4 Gb DRAM memory chips, embedding 8 processors on die

Delivered as standard DDR4 2400 DIMM modules with 16 chips

Server CPU helped by thousands of additional cores

Boosting 20x data intensive applications

Power efficiency 10x better

By reducing drastically CPU-DRAM data movement

At marginal cost

Source: HOT CHIPS 31, UPMEM 2019 Paper
RISC-V Application domain from edge to cloud

Andes V5 Adoption

Applications:
- ADAS
- AIoT at the edge
- Communication: BT, WiFi, 5G
- SSD: enterprise/consumer
- FPGA
- MCU
- Multimedia: A/V, AR/VR
- Block chain
- Datacenter AI accelerator
- Security

50% use AI

40nm to 7nm

Courtesy of: Andes Technology
RISC-V Application domain from edge to cloud

Andes just announced it achieved a record of 125 licensing agreements for its new family of RISC-V processors during the year of 2019 so far.

Courtesy of: Andes Technology
Contribution in Foundation Task Groups

RISC-V Taiwan Alliance (RVTA)
Contribution in software ecosystem

GNU Toolchains

RISC-V LLVM Porting Effort
- Alex Bradbury is in charge of RISC-V LLVM/M
  - Talk yesterday afternoon
  - Poster on Tuesday night
- RV32IM[A]FD support upstream
  - Missing hard-float calling convention
  - Missing 64-bit support
  - Missing 32-bit support
- Clang, Go, and OpenJDK have run code
  - Rust part in progress
  - Poster on Tuesday

RISC-V Linux Kernel Port
- Linux: January, 2018
  - Only RISC-V-based systems
  - Drivers are trickling in now
RISC-V in University research is growing

RISC-V Taiwan Alliance (RVTA)

National Cheng Kung University
National Chiao Tung University
National Taiwan University
National Sun Yat-Sen University
National Tsing Hua University
Taiwan Semiconductor Research Institute
RISC-V TAIWAN Alliance (RVTA) is committed to coordinating industry, academic, and research institute to work together and introduce RISC-V open architecture to Taiwan.

As soon as we connect resources from RISC-V ecosystems worldwide, Taiwan’s R&D, design and application will be capable of integrating AIOT and hitchhiking 5G trends and business opportunities, improving Taiwan’s industrial competitiveness.
Mission
RISC-V Taiwan Alliance (RVTA)

Market
Support Taiwan’s semiconductor business to enter the core customization of IC design and expedite the RISC-V open architecture into commercial market.

Technology
Promote RISC-V technology and accelerate the development of AIoT and edge computing industry in Taiwan.

Talents
Cultivate talents, and connect resources from RISC-V ecosystems worldwide, making Taiwan’s ICT industry a key player in the global supply chain and core AIoT solution provider.
Our Members
RISC-V Taiwan Alliance (RVTA)
What we have achieved

- Mar 7th, 2019
  RVTA was established

- May 22nd, 2019
  Chairman Wang visited MIIT in Beijing

- May 29th, 2019
  RVTA hosted the RISC-V forum at COMPUTEX TAIPEI

- Jul 30th & Sep 17th, 2019
  RVTA co-hosted cross-strait standards forum in RISC-V section
Community is a great force to advance technologies. But, you must be able to work with it and tolerate its pace.
THANK YOU!

www.tw iota.org/risc-v